Cross-Layer Thermal Reliability Management in 3D Integrated Heterogeneous Processor for Breaking the Power and Bandwidth Walls

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Objectives
- 3DHP (3D integrated Heterogeneous Processors) is emerging as a key enabling tech for parallel and scalable heterogeneous computing.
- Objective is to address thermal and reliability integrity issues in 3DHP through a holistic cross-layer approach.

Dynamic Thermal Reliability Management (DTRM) System
- Task assigned to the University of Mississippi as part of this collaborative research project.
- Goal is to reduce thermal hotspots and temperature gradients with minimal possible performance impact for typical workloads on 3DHP via smart thermal and reliability aware task scheduling.
- Leverage techniques such as DWGS (Dynamic Workgroup Scheduling), inherent redundancy (especially on GPU), DVFS (Dynamic Voltage Frequency Scaling), PG (Power Gating).
- Experiments are performed using simulators such as Multi2Sim, McPAT, and HotSpot.

GPU Power Modeling
- Critical for building a realistic and accurate DTRM system.
- Goal is to design a configurable framework to model power and heat dissipation at architectural level.
- Detailed hardware statistics are generated by a cycle accurate architectural simulator called Multi2Sim.
- Power consumption data is generated by McPAT using the generated hardware statistics from Multi2Sim.
- Resulting power consumption data is turned to heat profile by a tool called HotSpot.

Approach

<table>
<thead>
<tr>
<th>Layer (Lead PI)</th>
<th>Issue</th>
<th>Proposed Approach</th>
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<tbody>
<tr>
<td>Runtime Layer</td>
<td>Need for dynamic runtime management for fine-grained runtime</td>
<td>DTRM (dynamic thermal reliability management)</td>
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<tr>
<td>Architecture</td>
<td>Spatially and temporally varying error rate induced by hotspots</td>
<td>Adaptive EDAC (Error Detection &amp; Correction) &amp; DRAM refresh engine for reliable storage and transfer of data among CPU, GPU, and DRAM dies via TSVs</td>
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<tr>
<td>Physical Layer</td>
<td>Need for on-chip offline sensing for thermal and mechanical integrity</td>
<td>Distributed temperature and TSView co-sensor framework for 3D stacked CPU+GPU+DRAM heterogeneous processor</td>
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Current Progress
- Initial framework for GPU power & heat modeling and heat map visualization are completed.
- Several OpenCL workloads have been ported and developed for the proposed DTRM.
- CPU and memory power modeling are under development.
- Integration of CPU, GPU, and Memory to emulate 3DHP is under planning.

Heat Map Visualization
- Visualize heat map at specific clock cycle while taking into account the interactions across vertical stacks (e.g., CPU and GPU, GPU and Memory).

Future Works
- DTRM software layer will be designed and implemented.
- Power model will be verified.

Current Products
1. Mainul Hassan, "Power and Hotspot Modeling for Modern GPUs," MS Thesis, The University of Mississippi

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