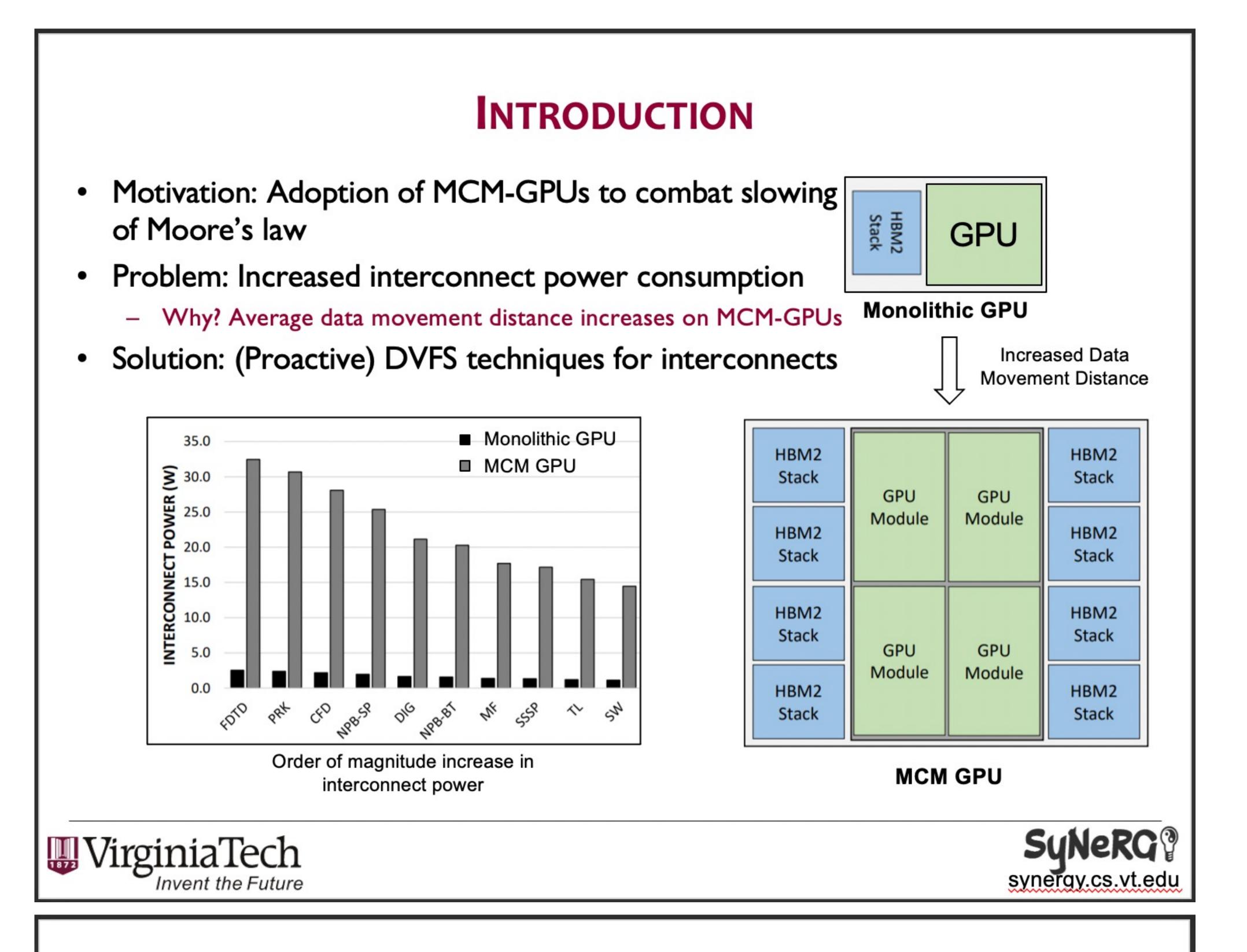
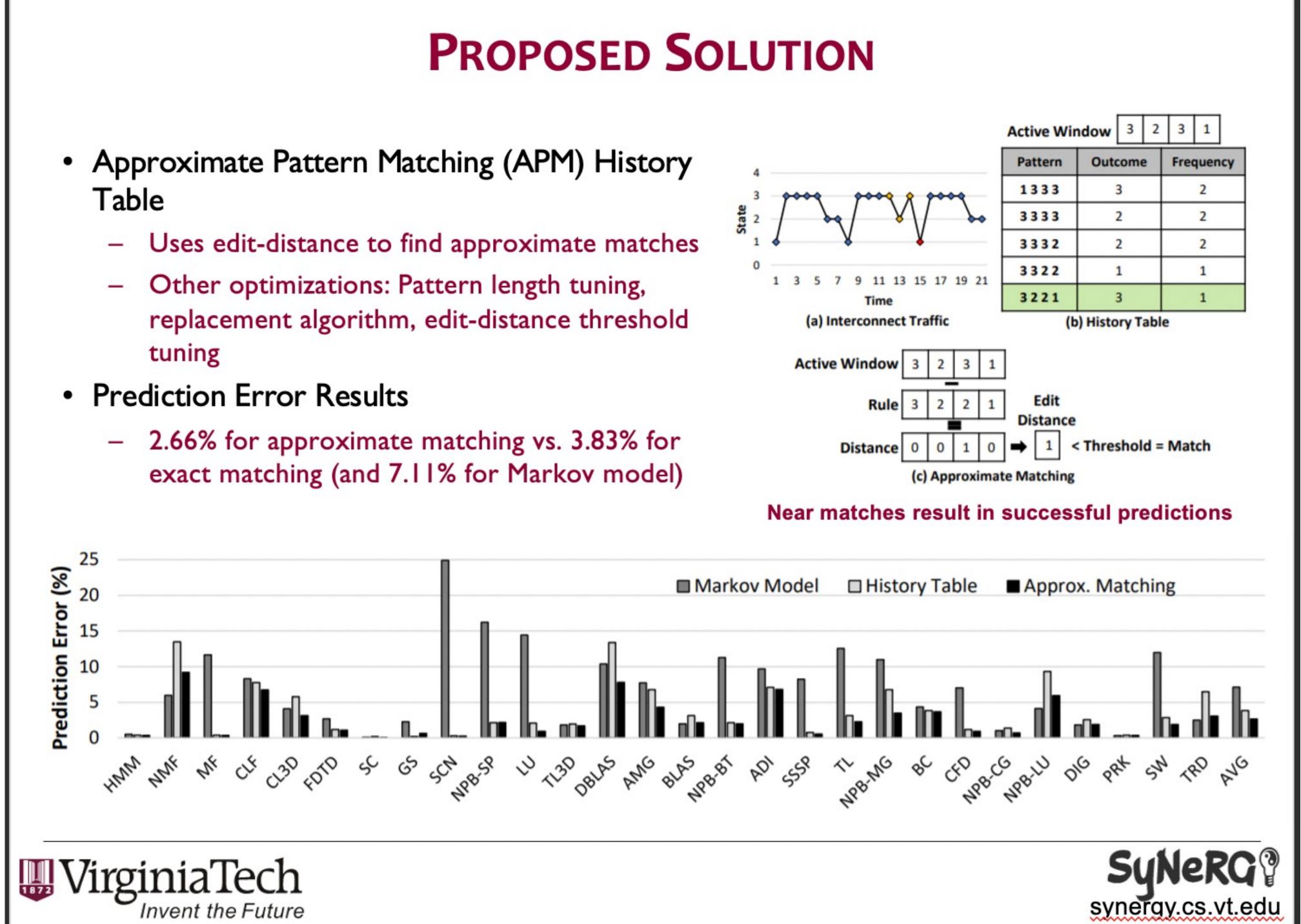
Approximate Pattern Matching for On-chip Interconnect Traffic Prediction

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PROACTIVE POWER MANAGEMENT **Approach** Predict interconnect traffic for upcoming kernels from past history Set interconnect's P-state based on expected traffic Phase prediction techniques and limitations - Markov Model: Slow adaptation to global phase change - History Table: High mispredictions for applications with irregular traffic and noisy traffic **Active Window** for(i=0; i<1000; i++){ Repeating Data Outcome pre process(vec); Pattern dependent val1 = process(MatA); irregularity 1333 val2 = process(MatB); val3 = process(MatC); 3333 val4 = process(MatD); 3332 d1 = det(MatD); if(d1 == 0)3322 res = compute(MatA, MatB, MatC, vec); 3221 9 11 13 15 17 19 21 res = compute(MatA, MatB, MatD, vec); No Matches for multiple kernels Toy Example SyNeRG? WirginiaTech synergy.cs.vt.edu Invent the Future

NEXT STEPS

Conclusion

- Phase prediction via approximate pattern matching benefit kernels exhibiting irregular, non-uniform, noisy traffic
 - 3.83% error for state of the art → 2.66% for proposed approach

Next Steps

- Extensions to approximate pattern matching for different types of mismatches (e.g., inserts, deletes, and swaps)
- Hardware design and implementation to meet target latency (5us) and power budget (0.1W) for real-world adoption
- Application-level performance and power evaluations

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The authors thank Joseph Greathouse (AMD) for providing the input traces used in this study.



