

CoreTSAR: Core Task-Size Adapting Runtime

Thomas R.W. Scogland, *Student Member, IEEE*, Wu-Chun Feng, *Senior Member, IEEE*,
Barry Rountree, and Bronis R. de Supinski, *Member, IEEE Computer Society*

Abstract—Heterogeneity continues to increase at all levels of computing, with the rise of accelerators such as GPUs, FPGAs, and other co-processors into everything from desktops to supercomputers. As a consequence, efficiently managing such disparate resources has become increasingly complex. CoreTSAR seeks to reduce this complexity by adaptively worksharing parallel-loop regions across compute resources without requiring any transformation of the code within the loop. Our results show performance improvements of up to three-fold over a current state-of-the-art heterogeneous task scheduler as well as linear performance scaling from a single GPU to four GPUs for many codes. In addition, CoreTSAR demonstrates a robust ability to adapt to both a variety of workloads and underlying system configurations.

Index Terms—Heterogeneous, OpenMP, OpenACC, GPU, coscheduling

1 INTRODUCTION

WHILE heterogeneous systems are becoming more popular, their programming models deter many potential users. Unlike adding more or faster CPUs, where existing programming models work without code changes, programs must be explicitly updated to use GPUs and other accelerators. Rather than grapple with unfamiliar programming models, users often run their CPU-only code on accelerated resources, leaving a significant portion of the computing resources idle. Accelerated OpenMP, our term for a class of directive-based programming models including OpenMP for Accelerators [1] and the PGI accelerator model [2] among others, can ease this transition by allowing users to target accelerators with a familiar OpenMP-style syntax. However, Accelerated OpenMP is not a panacea: current iterations help one *move* their computation to a *single* accelerator with straightforward syntax. Once moved however, there is no way to workshare a loop across multiple devices without *manually* targeting each device.

In order to target, for example, a GPU and four CPU cores, a user must manually split the work, run that work on each separate device, and manually merge each result. Any load balancing, coherency, or runtime adaptation of any kind must be reimplemented by every user. So, while Accelerated OpenMP can parallelize serial code via annotation, it lacks the ability to scale and to load-balance work transparently on the hardware found at runtime.

Our work enables safe and efficient worksharing across devices in Accelerated OpenMP. To do so, we must address two primary concerns. First, we manage memory input and

output across multiple address spaces without requiring alterations to the associated parallel loop. Second, we divide work across devices with vastly different computational capabilities fairly and efficiently. In all, our CoreTSAR (Task-Size Adapting Runtime) library automates the scheduling, load balancing, and cross-device data management for safe and efficient worksharing. This paper presents the design and implementation of CoreTSAR and the extended Accelerated OpenMP syntax to integrate its functionality. Specifically, we make the following contributions:

- The design and syntax of a multi-target, worksharing construct for Accelerated OpenMP;
- The design, implementation, and optimization of our scheduling and memory management library, CoreTSAR, which can be used with any Accelerated OpenMP compiler/runtime or with CUDA and CPU OpenMP directly;
- Seven adaptive scheduling policies, spanning from a low-overhead but coarse-grained adaptive approach to a chunk-based, fine-grained scheduling approach for distributing work.
- A rigorous performance evaluation of CoreTSAR that demonstrates how runtime scheduling can significantly improve performance while maintaining programmability.

The rest of the paper is composed as follows. Section 2 offers motivation and background. Section 3 describes the design of CoreTSAR, including our task management concept, scheduling mechanisms, and memory management. Details on our implementation follow in Section 4. Section 5 present our results. Related work follows in Section 6 and conclusions in Section 7.

2 BACKGROUND AND MOTIVATION

As heterogeneous systems spread through the marketplace, so do programming models that target them. While a variety of programming models exist, most fit into one of three categories: (1) loop-offload models; (2) block-and-grid models; and (3) blocked-task models.

• T.R.W. Scogland and W.-C. Feng are with the Department of Computer Science, Virginia Tech, Blacksburg, VA 24060.
E-mail: {tom.scogland, wfeng}@vt.edu.

• B. Rountree and B.R. de Supinski are with the Center for Applied Scientific Computing, Lawrence Livermore National Laboratory, Livermore, CA 94551. E-mail: {routree, bronis}@llnl.gov.

Manuscript received 24 Mar. 2014; revised 25 Aug. 2014; accepted 30 Sept. 2014. Date of publication 26 Oct. 2014; date of current version 7 Oct. 2015.

Recommended for acceptance by Z. Tari.

For information on obtaining reprints of this article, please send e-mail to: reprints@ieee.org, and reference the Digital Object Identifier below.

Digital Object Identifier no. 10.1109/TPDS.2014.2365192

```

1 void runGemm(T **a_a, T **b_a, T **c_a) {
2     T *a = *a_a, *b = *b_a, *c = *c_a;
3     //OpenMP
4     #pragma omp parallel for
5     //Accelerated OpenMP
6     #pragma acc region for copy(c[0:N*N]) \
7         copyin(a[0:N*N],b[0:N*N])
8     //Accelerated OpenMP + extension
9     #pragma acc region for part_copy(c[1:N][0:N])\
10        copyin(b[0:N*N]) part_copyin(a[1:N][0:N])\
11        hetero(1, all, adaptive)
12        for (int i = 0; i < N; ++i) {
13            for (int j = 0; j < N; ++j) {
14                c[(i*N) + j] *= B;
15                for (int k = 0; k < N; ++k) {
16                    c[(i*N)+j] += A * a[(i*N)+k] * b[(k*N)+j];
17                } } }
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
841
842
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
860
861
862
863
864
865
866
867
868
869
870
871
872
873
874
875
876
877
878
879
880
881
882
883
884
885
886
887
888
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971
972
973
974
975
976
977
978
979
980
981
982
983
984
985
986
987
988
989
990
991
992
993
994
995
996
997
998
999
1000

```

Fig. 1. A basic GEMM kernel as implemented in OpenMP variants (top left), CUDA (bottom left) and OmpSs (right).

Loop-offload models include variants of Accelerated OpenMP [1], OpenACC [3] HMPP [4], PGI accelerator directives [2], and Intel OpenMP offload extensions for their Xeon Phi coprocessors. They extend an OpenMP-like annotated, serial, source model with data-movement declarations to offload work to a device with a distinct address space. The top left of Fig. 1 shows a basic molecular modeling kernel (GEMM) implemented serially with OpenMP, Accelerated OpenMP, and our proposed Accelerated OpenMP extensions. With no pragmas, the loop runs serially, as one would expect. The OpenMP pragma on line 4 workshares the loop across CPU cores. Accelerated OpenMP’s pragma (lines 6-7) adds explicit *in* copies of the *a* and *b* arrays and an *inout* copy of *c*. Each of these first two pragmas workshares the loop iterations across a single address space, *either* CPU cores *or* a single GPU. We discuss the third pragma at the end of this section.

Block-and-grid models include CUDA [5] and OpenCL [6]. These low-level models specifically target GPU-like hardware by offloading blocks or groups of threads to an array of cores, each of which is a SIMD unit. Generally these cores share memory with one another but not directly with the CPU. The lower left of Fig. 1 shows an example using CUDA. In addition to changing the array accesses, explicit memory allocation and copies are required to move data to and from the device. The loop is converted into a grid of threads, each of which executes a single iteration in the `cudaG()` kernel, which must be called with the number of blocks and threads per block. As with the loop-offload example, this code uses exactly one GPU.

Blocked-task models, like OmpSs [7] and StarPU [8], specify tasks and their dependencies in terms of blocks of

data (and sometimes other tasks). The right-hand code-block in Fig. 1 uses OmpSs to implement the GEMM kernel with load balancing across CPUs and GPUs, so it contains *both* CPU *and* CUDA kernels, both aliased to the `gemm()` function by the compiler. Each call to `gemm` is given the start address of the block, in this case a row, to process. These calls are converted into tasks, which are enqueued into the OmpSs runtime with their data. Each task can then be scheduled, individually, on any device an implementation is available for. Since the task size is *fixed*, each task must encompass enough work to occupy all compute units on a GPU long enough to amortize the overhead of scheduling it; on the other hand, each task must also be small enough not to overload a single CPU core.

Each programming model has its advantages and disadvantages. The block-and-grid approach (e.g., CUDA or OpenCL) is highly efficient on the GPU and offers maximum control over them. The loop-offload version requires the least change from serial or OpenMP code, but it offers less control. Blocked-task models offer control through direct use of the other models as well as automatic load-balancing across all compute resources. Unfortunately, they also require the greatest departure from the original code.

Therefore, we need a programming model that offers the performance of block-and-grid models, flexibility of blocked-task models, and programmability of loop-offload models. Our proposed extensions, along with our prototype library implementation, brings us closer to this goal by introducing work-sharing across devices to Accelerated OpenMP without requiring a specific task granularity from the user. The third pragma, in the upper left of Fig. 1 (lines 9-11) illustrates how our proposed extension would work-share the

```

//items in {} are optional
#pragma acc region \
  hetero(<cond>{, <devs>{, <sched.>{, <ratio>{, <div>{}}}) \
  part_copy{in/out}(<var>{(<size>){<cond>:<num>{:<halo>}}}) \
  persist(<var>)
#pragma acc depersist(<var>)

```

hetero() inputs

<cond>	Boolean, true=coschedule, false=ignore
<devices>	Allowable devices (cpu/gpu/all)
<scheduler>	Scheduler to use for this region
<ratio>	Initial split between CPU and GPU.
<div>	How many times to divide the iteration space

part_copy() and {de}persist() inputs

<var>	Variable to copy.
<size>	Size of each "item" in the array/matrix.
<cond>	Whether this dimension should be copied.
<num>	Number of items in this dimension.
<halo>	Number of halo elements required.

Fig. 2. Our proposed extension.

GEMM loop across an arbitrary number and type of supported devices. Thus, it offers more flexibility in the region than even blocked-task models, while maintaining the serial loop as written.

3 DESIGN

This section presents the design of our proposed extension, schedulers and memory management infrastructure. CoreTSAR safely divides annotated, un-blocked, serial loops, as used in many traditional OpenMP applications, and schedules them across heterogeneous resources. We add a clause to Accelerated OpenMP that is similar to the `schedule()` clause. The OpenMP programming model imposes the following constraints on our design:

- 1) Use existing, unchanged code in the Accelerated OpenMP loop region;
- 2) Treat the accelerated loop as a group of related tasks that are defined by the loop code and the region directive including its associated clauses;
- 3) Maintain data consistency outside of the region and do not alter data accesses in the existing loop body although we can extend the data copy clauses of the region.

By following these constraints we preserve programmability while adding significant new functionality.

3.1 The Proposed Extension

The CoreTSAR interface consists of two parts, which Fig. 2 depicts. The `hetero()` clause specifies how to schedule the region and which classes of device should be considered. For memory management, we add the `part_copy()` clauses to provide the runtime with sufficient information to partition input and output data for the region safely.

Our clauses are permitted on the accelerator directive or on any top-level accelerator loop construct, with the same restrictions as existing accelerator loop constructs. Specifically there must not be inter-iteration dependencies other than those handled by reductions. Unlike normal copy clauses, `part_copy` is not allowed on data clauses as it only has meaning when directly associated with a loop. We still support data regions, but only for cases

where complete replication of the input/output is desired, as opposed to only those data regions that are required. We define the properties of our clauses in greater detail in the following sections.

3.2 Scheduling

In order to workshare the iterations in a given region efficiently, we must offer appropriate scheduling policies. Each policy in CoreTSAR treats the iterations within a loop region as a group of related tasks, which allows us to select the scheduling granularity adaptively. For example, CoreTSAR can break a region with 10,000 iterations into four chunks or a thousand or any number less than 10,000 for scheduling, without modification and without user intervention. This capability is critical for efficiently scheduling across heterogeneous systems, as a single grain size is rarely appropriate for all available devices.

Existing OpenMP schedules for CPUs divide the iteration space either evenly across processors statically or into *chunks* that are assigned dynamically. The static version is simple, efficient to implement, and consistent, but does not load-balance. Alternatively, OpenMP's chunk based schedules (*dynamic* and *guided*) load-balance well in homogeneous architectures. However, they suffer high overhead due to synchronization at each work-request and especially as a result of the lack of data locality their dynamic algorithms cause. In heterogeneous systems they would also incur repeated kernel launches and data transfers. We dealt with these issues in our initial work with CoreTSAR [9], by designing a set of adaptive schedules that statically divide the work within each pass through a region but load-balance across passes. This scheme proved effective, but it does not tolerate imbalanced workloads well, whereas chunk-based schemes can. To address that case and broaden our evaluation, we have developed a number of new chunk-based designs as well as a hybrid of the two approaches.

3.2.1 Static/Adaptive Schedulers

Our static and adaptive schedulers [9], [10] predict the time that each device will take to complete an iteration in the next pass and generate a single task for each device sized such that all finish the region as close to simultaneously as possible. These schedulers make two assumptions: (1) the average runtime of an iteration in the region is constant on a device; and (2) subsequent passes through the region have the same performance ratio as the previous pass. Also, our schedulers begin with a default time per iteration for each device until we have gathered runtime data. This default is either a user-defined value, one saved from a previous run, or one based on the formula $1/(\text{deviceSIMDWidth}/\text{baseDeviceSIMDWidth})$. While we do not claim that this formula accurately models the relative performance of devices, in practice we have found it to be accurate for dense floating-point kernels. We leave further exploration of default values as future work.

The linear program in Fig. 3 uses the time per iteration value for each device to calculate the fraction of the total available iterations that should be allocated to each device. In words, the program finds the fractions of work that result in the minimum deviation between predicted execution

$$\begin{aligned}
 I &= \text{total iterations} & \min(\sum_{j=1}^{n-1} t_j^+ + t_j^-) & \quad (1) \\
 i_j &= \text{iterations for} & & \\
 & \text{compute unit (CU) } j & & \\
 f_j &= \text{fraction of iterations} & \sum_{j=0}^n f_j &= 1 \quad (2) \\
 & \text{for CU } j & & \\
 p_j &= \text{recent time/iteration} & f_2 * p_2 - f_1 * p_1 &= t_1^+ - t_1^- \quad (3) \\
 & \text{for CU } j & f_3 * p_3 - f_1 * p_1 &= t_2^+ - t_2^- \quad (4) \\
 n &= \text{number of CUs} & \vdots & \\
 t_j^{+/-} &= \text{time over/under equal} & f_n * p_n - f_1 * p_1 &= t_{n-1}^+ - t_{n-1}^- \quad (5)
 \end{aligned}$$

Fig. 3. Our adaptive scheduler's deviation minimization algorithm as a linear program, variables at left.

times. (Our initial version of this linear program calculated the optimal number of iterations directly as an *integer* solution, giving theoretically optimal splits based on our model. This integer solution, however, was impractical to run online due to high calculation costs.) The linear program formulated in Fig. 3 dramatically reduces the calculation costs and is designed to still yield an optimal fractional result, allowing the solution to be off by up to one iteration on each device but decreasing the computation time by several orders of magnitude.

Our *static* schedule applies this linear program to the default, or supplied, values once at the beginning of the first pass through a region, then reuses the result thereafter. The adaptive schedules (*adaptive*, *split* and *quick*) use a first pass with the static schedule as a training phase. The first time that we encounter a CoreTSAR region, we assign work based on the static schedule and then measure the times on each device. For each following scheduling decision, we use measured times per iteration in the linear program, converging on a more efficient schedule. Our design intentionally includes all recurring data transfer and similar overheads required to execute an iteration on a particular device, naturally incorporating data transfer and launch overheads.

Adaptive trains on the first full pass through the region, then adapts at the beginning of each subsequent pass. *Split* is designed to adapt within regions that either cannot tolerate a full pass with a poor schedule, or only run once per application run. *Split* breaks each pass into several evenly split subpasses, based on the `div` input. It treats each subpass as the same as a full pass with *adaptive*. While *split* provides better, and earlier, load-balancing for some applications, it increases overhead in each pass. *Quick* balances between *split* and *adaptive* by executing a small subpass for its first training phase, similarly to *split*. It then schedules and runs all iterations remaining in the first pass, and uses the adaptive schedule for all subsequent passes. This schedule suits applications that cannot tolerate a full pass using the static schedule or the overhead of extra scheduling steps in every pass.

3.2.2 Chunk Schedulers

Chunk schedulers are exemplified by the OpenMP *dynamic* schedule, in which a chunk size specifies the number of iterations assigned to each thread each time it requests work. These schedulers effectively use a work queue approach, which offers natural load balancing. While it is a classic

load balancing approach, it is most effective when used with homogeneous computing resources with fast synchronization mechanisms, which is not the environment that CoreTSAR targets. Thus, we present variations on this method for hybrid systems.

Specifically, we design three new schedules (*chunk*, *chunk static* and *chunk dynamic*). *Chunk* serves as our baseline chunk scheduler, and is functionally identically to OpenMP's *dynamic* schedule. *Chunk static* scales the chunk size for each device based on the same scheme used in the *static* schedule above. Thus, larger chunks are provided to devices with greater compute power. Finally, *chunk dynamic* begins in the same way as *chunk static* then dynamically adapts the chunk size for each device based on their performance. Unlike the adaptive schedulers, it does not employ the linear program to determine the new chunk size since the chunk schedulers do not have a natural barrier point where all times have been updated. Instead, it employs an annealing approach that computes a weighted average of the time per iteration for each device, and attempts to reduce the time per iteration by increasing or decreasing the chunk sizes. For example, if the time per iteration on a device decreases with an increased chunk size, *chunk dynamic* again increases that chunk size. In this design, each device is independent and does not block on the others in order to adapt.

3.2.3 Hybrid Scheduler

In addition to the schedulers that are strictly chunk or ratio based, we also investigate a *hybrid chunk* schedule that begins as a *chunk dynamic* schedule and after the first pass transitions into the adaptive scheduler. *Chunk dynamic* adapts and load balances quickly during the first pass while refining the split. However, after that first pass, it incurs unnecessary overhead in contention and memory transfers, where adaptive excels. Using *chunk dynamic* in place of *static* for the training phase of *adaptive* naturally fuses the advantages of both schedulers.

3.3 Memory Management

In order to maintain memory coherency across address spaces while dynamically splitting the region, CoreTSAR requires information about the memory access pattern of each iteration of the loop. The primary design goal of our memory manager is to support unblocked input and output data naturally. Our interface covers the majority of common dense storage cases, and can be used at some memory overhead with various more complex or sparse schemes, while a method to specify any possible association is an ongoing topic of research, including our future work. As we discuss in Section 4, our prototype library implements the memory management for all examples evaluated in Section 5.

For each variable the `part_copy()`, or partial copy, interface requires at least a variable name, one dimension to copy, and the number of items in that dimension. Given the clause `part_copyin(a[1:N])`, `a[i]` will be copied, where `i` is the current loop iteration, to the device that executes that iteration. If a range of `i` from 5-500 is assigned to a device, `a[5-500]` will be copied. Thus, the partial copy is associated with the loop iteration(s) of the loop being split.

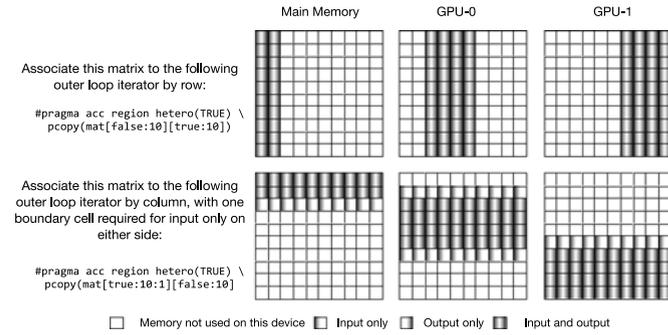


Fig. 4. Example memory association patterns, assuming a pass in which two iterations are assigned to the CPU device, and four each to two GPUs.

Fig. 4 displays two simple examples of patterns produced by our memory-association syntax. The top example specifies that a 10×10 matrix is being registered to the region, and the iterator will be associated with the column dimension, assuming C ordering, since the column dimension's condition is true. The lower example selects the row dimension instead, and additionally specifies that one halo element is required on either side of that dimension. This pattern is typical of stencil-type computations, where halo values are required as input, but are not updated by the device reading them, having the halo argument makes supporting such associations natural.

Our interface does not directly support random access output, reverse indices or indirect indices. For input, these can all be supported at the cost of additional overhead by copying the entire data set, since the input process is non-destructive.

3.4 Example Usage

Fig. 5 shows how to use our proposed interface to implement the example in Fig. 1. All options, including those that use default values, are specified for `part_copyin(a...)` and `hetero(...)` in the example. The minimum necessary to specify the copy correctly are used for `part_copy(c...)`. In this example, the loop will always be split across devices using the adaptive scheduler with the default ratio and a div of 10. The copies specify that the `a` array is two-dimensional, of size `N` by `N`, made up of elements of size `sizeof(T)`, and that iteration `i` requires row `i` of `a` but not column `i`. The `c` copy specifies the same as for `a` except that it should be copied both in and out. The traditional `copyin()` clause from accelerated OpenMP is used for `b` since all participating devices need access to the full region. Complete output, in the form of `copyout()`, is not allowed however because there is no way to resolve the changes between versions. We may investigate this in future work.

4 IMPLEMENTATION

We implement CoreTSAR as a C library on top of Accelerated OpenMP, tested with PGI Accelerator and Cray's Accelerated OpenMP. Our evaluation in this paper focuses on PGI Accelerator, so our examples use its directive format. This section discusses our implementation including its portability, API and our memory manager as well as some necessary deviations from the design discussed in Section 3.

```

void runGemm(T **a_a, T **b_a, T **c_a) {
    T *a = *a_a, *b = *b_a, *c = *c_a;
    #pragma acc region for part_copy(c[1:N][0:N]) \
        part_copyin(a[1:N:0][0:N:0]) copyin(b[0:N*N]) \
        hetero(1, all, adaptive, default, 10)
    for (int i = 0; i < N; i++) {
        for (int j = 0; j < N; ++j) {
            c[(i * N) + j] *= B;
            for (int k = 0; k < N; ++k) {
                c[(i*N) + j] += A * a[(i*N) + k] * b[(k*N) + j];
            }
        }
    }
}

```

Fig. 5. Our proposed extension to accelerated OpenMP.

4.1 GPU Back-Off

Some applications are not amenable to being run on GPUs, or at least the GPUs present in some systems. While iterations of a region may benefit greatly from running on an NVIDIA c2075, they may perform poorly on an NVIDIA GeForce GT 520. In order to maintain portability across disparate accelerator and CPU capabilities, CoreTSAR implements GPU Back-off support in all adapting schedulers.

The back-off system is implemented differently for each of the two scheduler types. In the adaptive schedulers CoreTSAR converts a GPU offload thread into a CPU thread when the GPU has a higher time per iteration than the slowest CPU core for a configurable number of passes (default is two). We use multiple iterations since under certain circumstances, such as loading large persistent datasets for the first time, or an inappropriate initial amount of work, a device can be erroneously classified as slower than the CPUs. With the chunk schedulers, we base the decision on whether a given GPU completes fewer iterations than the slowest CPU core during each pass of a configurable number of passes. This difference compensates for the sometimes highly variable time per iteration when bootstrapping chunk schedulers across initial data copies, which can cause false conversions with the adaptive back-off scheme. We discuss the effects of this extension further in Section 5.

4.2 Memory Management

The existing memory interface of Accelerated OpenMP is insufficient to express the relationships necessary to handle certain kinds of memory association. While accelerated OpenMP does natively support copying a subset of an array, it does not support copying multiple subsets of one array, nor does it support non-contiguous rectangular sections such as a subset of the columns of a 2D array.

In order to support our desired memory association interface, CoreTSAR implements its own memory manager, using the `deviceptr()` clause to pass CoreTSAR managed memory into Accelerated OpenMP regions. We offer a straightforward syntax by which users specify the data required by a given iteration. Given that information, CoreTSAR automatically copies the ranges of data required by whatever iterations are assigned to a given device for that pass. When possible the memory manager uses pinned memory to accelerate copies, as well as asynchronous copies to and from the device in order to overlap them with scheduling and synchronization.

Currently, the CoreTSAR memory manager handles a restricted set of partial copies. In addition to the straightforward one-to-one relations, CoreTSAR also supports stencils through padding, and row, column or planar associations on two and three dimensional matrices. In order to support reductions we provide an API inspired by user-defined reductions in OpenMP 4.0. We discuss the details further in Section 4.4. While only a subset of the possible cases, these mappings are sufficient to implement all benchmarks evaluated in this paper.

4.3 Data Packing and Padding

Our original implementation of the memory interface [9] had a material weakness. That version of CoreTSAR allocated the full size of each memory region on each device in order to preserve offset accuracy. In other words, any input or output array/matrix supplied to CoreTSAR was allocated in full in all participating address spaces. Managing subset allocation and access without invalidating offsets and iterator values is a difficult problem, especially in languages like C.

We have redesigned CoreTSAR to support three kinds of regions depending on how the data is mapped. The first, and most simple, case is a one dimensional partial array or two dimensional array that is associated by rows. Since all of the resulting subsets are contiguous, the runtime provides an offset pointer that can be indexed by the original offsets without issue. No further action or overhead is required for this case, and a significant amount of storage on accelerators can be saved. The second case is where a two or more-dimensional array is associated by columns. CoreTSAR can pack these, but must have control over the calculation of offsets into the resulting matrix. As such, we handle this case in our translator for contiguous arrays accessed with `array[i][j]` style syntax, but currently do not support dynamically-allocated C arrays accessed with the `array[i*row_size + j]` syntax, though these can be supported by directly using the C API functions. Third, associations can use both the row and column associations, resulting in a region resembling a plus-sign being assigned to each device. Since these require the full range in both rows and columns, even though they may not need the corners, CoreTSAR is forced to allocate the full size of such arrays.

By allowing data regions to be packed, CoreTSAR gains two extra capabilities beyond reducing memory usage on target devices. The packing functionality allows any chunk-based scheme to place a low bound on memory use by selecting a small chunk size. This allows large data sets on the host to be streamed through accelerators without enough memory to hold even their assigned sub-part of the problem. When used in this mode however, CoreTSAR becomes similar to a blocked-task system, including the increased task management and data-transfer overhead that implies.

Perhaps more importantly however, the capability to adjust indexing, as described for column-wise associated multi-dimensional arrays, allows regions not only to be shrunk to save space, but also padded for alignment. As is well known, memory alignment is important for the

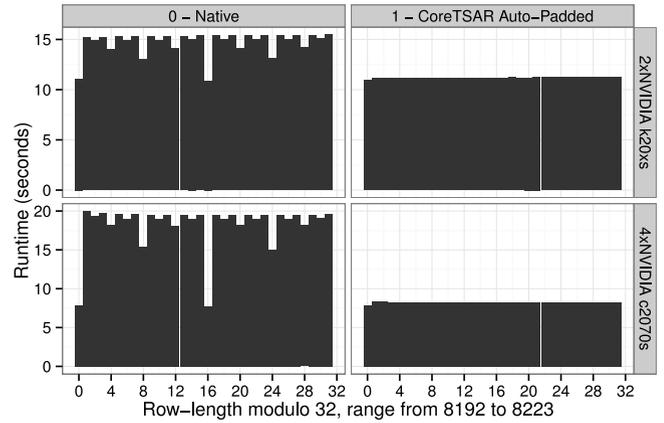


Fig. 6. Runtime of GEMM kernel on square matrices, statically scheduled across GPUs only with and without auto-padding.

performance of SIMD computations and coalesced memory accesses are important to the performance of GPU kernels. Given the ability to pad rows beyond the data assigned to each device, or even rows of data that are mis-aligned by the user, CoreTSAR can ensure that each row is aligned for most efficient access on each target. We implement this optimization by ensuring that the length of each row in a matrix is a multiple of the target device’s SIMD width. While in some cases this choice is more strict than required, it is consistently sufficient to ensure reasonable alignment.

Fig. 6 shows the effect that even small changes in row-width can have on performance without padding, and how our auto-padding helps. The figure represents the performance of a general matrix multiplication kernel when run with row and column lengths ranging from 8,192 to 8,223 elements in increments of one, specifically the x -axis values are the number of elements over 8,192 in each row. On our primary evaluation system, with four c2070 GPUs, a square matrix of size 8,192 \times 8,192 runs in 7.9 seconds. Increasing that size by only one element on each side more than doubles that runtime to 19.5 seconds. In fact, every odd-numbered increase in size takes approximately the same increased time, while each power of two increase does better up to 16, or a total of 8,208, which performs the same as the original 8,192. Another system with a pair of k20x GPUs shows a nearly identical stepped pattern as well. The difference in performance is somewhat smaller, ranging from 10.9 seconds at the zero and 16 positions and 15.2 at the odd offsets. The L2 read request performance counters provide a partial explanation for the wide range in performance. When padding is enabled, the difference in L2 requests with a multiple of 16 row length is consistently within 10 percent; for any odd length it balloons to 80 percent more L2 accesses for the un-padded version. This increase is due to a greater number of reads being required to accommodate the mis-aligned read requests of each warp on the GPUs, increasing contention and lowering cache efficiency overall. On the right-hand-side of the plot, you can see that CoreTSAR’s automatic padding smooths out these issues. Also, when dividing a data-set column-wise, this padding support can ensure alignment even when the appropriate amount of work to be assigned is not a multiple of the target device’s native SIMD width, an important consideration for several of our benchmarks.

4.4 CoreTSAR API and Usage

This section describes the low-level API to the CoreTSAR library in detail.

ctsar_init. Initializes an instance of the CoreTSAR runtime, one such instance should be used for each region that is to be separately scheduled. The parameters allow a user to set the default scheduler, allowed devices, the default time per iteration for each accelerator as an array of doubles (NULL for defaults), and how finely the split and quick schedulers should divide regions (NULL for default).

ctsar_next. Computes the division of work for the region associated with *c* based on size total iterations. This function is also responsible, updating appropriate memory regions on each target device and starting timers to evaluate each device's performance.

ctsar_loop. In order to support *split*, *quick* and the chunk schedulers, CoreTSAR must reevaluate the loop with each thread repeatedly. The *ctsar_loop* function serves as the condition for a do/while loop surrounding each region. In addition to managing repeats, the loop function is responsible for synchronization, GPU back-off support, copying data back from all devices, completing reductions, and calculating performance statistics at the end of each pass.

ctsar_reg_mem_{2d}. These functions register a host buffer with CoreTSAR. The full version takes a pointer to CPU memory, the size of an element of the input data, the number of element in each row/column, the number of halo elements required, and a flag option that allows the user to control copy direction and type. The non-2D version is shorthand for 1D arrays. The return value is a pointer to the memory assigned to the calling thread, which may or may not be identical to the original pointer.

The flags value controls whether memory is copied in or out or both, as well as whether to copy persistently, partially by rows or partially by columns and whether padding is to be allowed, if it is, an extra output parameter for the new row size is required. Partial copies are integral to the correct functioning of CoreTSAR as they make automatic merging of output possible. They also improve performance of input operations. The 2D interface supports all specifications discussed in Section 3, except that it does not handle matrices with dimensionality higher than 2.

Regardless of the flags, CoreTSAR allocates an appropriate size buffer on the device associated with the calling thread. If the region is set to persistent, data is immediately and asynchronously copied from the CPU array into the newly allocated memory, where it resides until it is explicitly removed with a call to *ctsar_unreg_mem()*.

ctsar_unreg_mem. De-registers the pointer from the region instance, frees the memory that stores the state of the data, and frees persistent regions.

ctsar_retarget_mem. Re-target allows a user to specify that the region already allocated for pointer *old* should be used to store the data pointed to by *new* on all devices. A typical use is to swap buffers for double buffering, although it can also be used to implement blocked data transfers by re-targeting a pointer to the new start pointer before entering a region.

ctsar_reg_reduc. This function registers a reduction. Because each memory space will have its own reduction result, CoreTSAR must safely initialize the temporary variables in each memory space and combine those results into a

```

void runGemm(T **a_a, T **b_a, T **c_a) {
    ctsar * s = NULL; int div = 10;
    ctsar_init (&s,N,CTSAR_ADAPTIVE,CTSAR_DEV_ALL,NULL,&div);
    #pragma omp parallel default(shared)
    do{
        T *a = ctsar_reg_mem(s, a_a[0], sizeof(T)*N, N,
            CTSAR_MEM_PARTIAL | CTSAR_MEM_INPUT);
        T *b = ctsar_reg_mem(s, b_a[0], sizeof(T)*N, N,
            CTSAR_MEM_INPUT);
        T *c = ctsar_reg_mem(s, c_a[0], sizeof(T)*N, N,
            CTSAR_MEM_PARTIAL | CTSAR_MEM_INOUT);
        ctsar_next(s,N);
        #pragma acc region for deviceptr(a,b,c) independent \
            if(ctsar_get_type(s) == CTSAR_DEV_GPU)
        for (int i = CSTART(s); i < CEND(s); ++i) {
            for (int j = 0; j < N; ++j) {
                c[(i * N) + j] *= B;
                for (int k = 0; k < N; ++k)
                    c[(i*N) + j] += A * a[(i*N) + k] * b[(k*N) + j];
            }
        }while(ctsar_loop(s));
    }
}

```

Fig. 7. CoreTSAR library version of GEMM.

meaningful final value. The identity pointer points to an appropriate initial value to use on each device. For example, in a sum the identity would usually be 0, in a product 1, and so on. The *item_size* specifies the size of the elements to be reduced. The *reduc* argument is function pointer that should accept two void pointer arguments, the first of which is both a value to be reduced and the output, the second is another value to be reduced. This function is called repeatedly to accumulate the final value as each device finishes execution. For simple reductions, the body of the function can be as simple as $*((int*)a) += *((int*)b)$.

CSTART/CEND. Macros used to retrieve the start and end values to use for iteration in the loop region.

Fig. 7 presents an example using this interface to implement the extension as presented in Fig. 5. In this example, CoreTSAR is initialized with the adaptive scheduler, default ratio, and div of 10. The parallel do-while loop allows our library to reevaluate the code region as necessary by looping with the *ctsar_loop(s)* call until done. The data regions are registered, as partial input, complete input, and partial input/output, and the appropriate pointers for those data regions on each device are returned into the local copies of pointers *a*, *b* and *c*. The *ctsar_next()* call calculates the number of iterations to be completed in this pass by each device. Once it is complete, the *CSTART()* and *CEND()* macros return the appropriate iterator range values for the device that evaluates them. This syntax can either be used manually, or generated by our python/libclang-based source-to-source translator.

While the code is extended significantly around the loop, we do not replicate or alter any code in the loop body. The Accelerated OpenMP *if()* clause determines if a thread runs on a GPU or CPU core. If the device is a CPU, the loop is run serially on the associated core completing its assigned iterations. If it is a GPU-controlling thread, the *acc region* directive workshares the assigned iterations across the associated GPU. All codes used in our evaluation are implemented in this fashion.

5 EVALUATION

This section evaluates the CoreTSAR library. We compiled all benchmarks with the PGI Accelerator compiler compiler

TABLE 1
Test System Specifications, All CPUs and GPUs Are Made by Intel and NVIDIA Respectively

System name	CPU Model	CPU Cores/die	CPU Dies	CPU RAM (MB)	GPU Model	GPU Cards	GPU Cores	GPU RAM (GB)
amdlow3	E3300	2	1	2,012	Tesla C2050	1	448	3
armor1	E5405	4	2	3,964	GeForce GT 520	1	48	1
dna2	i5-2400	4	1	7,923	GeForce GTX 280	1	240	1
escaflowne	X5550	4	2	24,154	Tesla C2070	4	448	6
hokiespeed	E6545	6	2	24,154	Tesla M2050	2	448	3

suite version 12.9. Optimization flags are `-acc -ta=nvidia -O3 -mp=allcores`. Table 1 lists our test platforms. Unless otherwise specified, tests were run on `escaflowne`. In tests with GPUs enabled, one CPU core is used to control each selected GPU and does not do computation. We use default scheduler parameters unless otherwise specified, with the initial split calculated at runtime based on the available resources and a div of 10. We include all scheduling overhead, GPU data transfer time, and synchronization time in all measurements.

Reported times and speedups include all activity that the original OpenMP CPU code did not require, such as library initialization, scheduling, and memory movement. We do not include application IO or problem setup that is shared between CPU, GPU and scheduled versions. We also record the time for each device to complete its assigned iterations, from which we can compute the time that devices wait for others to complete, the time spent to calculate the split for the next pass and, as a subset of that, the time to solve the linear program. Finally, we track the time per iteration for each device, as described in Section 3.

5.1 Benchmarks

We use four applications and the PolyBench/GPU [11] benchmark suite in our evaluation. CG [12] is a direct port of the NAS conjugate gradient benchmark. GEM [13] is a molecular modeling application for the study of the electrostatic potential along the surface of a macromolecule that has been extensively studied for GPU optimization [14]. Helmholtz is a discrete finite difference code that uses the Jacobi iterative method to solve the Helmholtz equation. K-means is a popular iterative clustering method. Our implementations of the 15 PolyBench/GPU benchmarks execute each computational kernel 10 times to mimic use in an iterative scientific application more closely. Tests at five and 15 kernel executions yield similar relative results. Since we are evaluating scheduling behavior, and not computational kernel performance, we made minimal changes in porting each benchmark. As such, our computational kernels are not optimized for the GPU other than by the compiler. Nonetheless, CoreTSAR can easily support optimized implementations through the same syntax.

For our purposes, benchmarks can be characterized by the number of passes through the parallel region that they make, the length of each of these passes, and how suitable they are to run on the GPU. Table 2 characterizes these properties for each benchmark. The table exhibits a wide range in number of passes through the parallel region -1 to 1,900 passes in the applications, and as high

as 10,240 passes for the GRAMSCHMIDT benchmark. Our adaptive scheduler operates primarily at the boundaries of parallel regions, so this number can greatly affect our results. For example, in the GEM benchmark, the adaptive schedulers are identical to the static scheduler because the training pass is the only pass in the application. Conversely, CG performs many short passes, which allows CoreTSAR to adjust scheduling decisions but incurs high scheduler overhead and data copy costs.

The table also shows a wide range of performance ratios. Values range from a $10\times$ slowdown to a $113\times$ speedup going from eight CPU cores to one GPU. Running GEM on only one GPU finishes the problem more than $10\times$ faster than on eight server class Intel CPU cores. CORR and COVAR also show extreme suitability, largely due to the static schedule employed in the CPU tests. Because the workloads are imbalanced, each CPU core performs a different amount of work. The GPU test, because of the load-balancing effect of over-provisioning work-groups on GPUs, handles this variation better. If we use the OpenMP dynamic schedule, COVAR runs in approximately 150 seconds, $10\times$ faster than the static performance. Alternatively, GRAMSCHMIDT and Helmholtz are not suited to GPU computation according to these results. Generally, the suitabilities match our expectations, with the exception of CG. Our previous work, and that of others, has found that CG is

TABLE 2
Benchmark Characteristics, Times in Seconds, Time/Pass for Static Schedule with CPUs and One GPU

Benchmark	Passes	Time/pass	CPU time	GPU time	Speedup on 1GPU
CG	1900	0.045	16.31	92.37	0.17
GEM	1	5.336	71.05	5.65	12.59
Helmholtz	50	0.138	1.18	7.22	0.16
kmeans	7	0.583	5.70	4.33	1.32
ATAX	10	0.646	32.23	6.60	4.88
BICG	10	0.822	21.86	8.78	2.49
CORR	10	0.162	157.73	1.64	96.07
COVAR	10	1.328	1558.30	13.80	112.90
FDTD2D	5000	0.000	0.99	1.23	0.80
GEMM	10	1.262	301.34	3.04	99.18
GESUMMV	10	1.902	2.10	20.38	0.10
GRAMSCHMIDT	10240	0.004	4.21	40.38	0.10
MVT	10	0.058	1.62	0.60	2.72
SYR2K	10	1.461	14.39	15.53	0.93
SYRK	10	0.769	7.86	8.18	0.96
THREEDCONV	10	1.031	5.77	10.95	0.53
THREEMM	30	0.284	126.03	3.78	33.35
TWODCONV	10	0.607	2.86	6.46	0.44
TWOMM	10	1.445	204.66	6.32	32.41

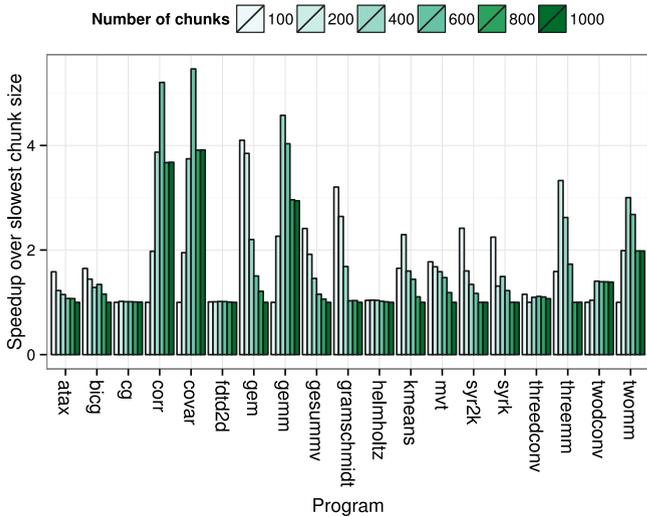


Fig. 8. Performance across chunk sizes for each benchmark with the basic Chunk scheduler.

suitable for GPUs. Some of our experiments on other platforms showed a ratio of approximately 0.55 on one GPU. Here, the GPU version takes more than $5\times$ longer than the CPU version. This is due to the high cost of data re-distribution across GPUs each iteration. We leave optimization of CG to future work.

5.2 Input Parameters

As mentioned above, we use the default values for our tests unless otherwise specified. However, chunk size does not have an obvious default. Fig. 8 illustrates the performance for the basic chunk scheduler across chunk sizes for each benchmark using one GPU. We do not report chunk sizes in terms of absolute iterations, which has little meaning across benchmarks. Instead, we compare by the number of chunks into which the region is partitioned. The performance of some applications varies little based on chunk size. Others, such as CORR and COVAR, have a range of as much as $3\times$. These ranges shift or even reverse in some cases as the number of GPUs or scheduler changes, creating even more variability. Due to the sensitivity to this parameter, all subsequent results for chunk-based schedulers use the best chunk size for that benchmark, scheduler, and GPU count combination.

5.3 CoreTSAR Performance

We begin with an evaluation of the overall speedup achieved for benchmarks across schedulers and GPU counts on escaflowne, as Fig. 9 depicts. All plots are based on the speedup over a chunk-based CPU schedule equivalent to OpenMP's dynamic schedule across the eight CPU cores. We can group these results roughly into three groups of behavior: those that scale to all four GPUs; those that benefit from GPUs but do not scale to more than one; and GPU-averse applications.

5.3.1 GPU Amenable Applications

Eleven benchmarks scale to four GPUs on escaflowne, resulting in between $3.5\times$ and nearly $200\times$ speedup. First GEM, GEMM, kmeans, SYRK, SYR2K, TWOMM and

THREEMM scale nearly linearly from one to four GPUs, missing linear only because of the use of one CPU core for the addition of each GPU. Slightly off of linear are CORR and COVAR, which gain performance at approximately one quarter of that rate, but consistently up to all four GPUs. Also in this group are ATAX, BICG, and MVT, which clearly taper off after two GPUs, since these benchmarks do not have enough work available at this problem size, to occupy all four GPUs fully. Further, we cannot increase the problem size without overflowing the GPU memory due to the way CoreTSAR's memory model currently handles mappings. In another peculiarity of these three benchmarks, the chunk scheduler performs almost identically to the CPUs. While all three reap significant performance benefits when run on GPUs, they are the only benchmarks that use column-wise partial copies. The overhead of column-wise copies for each chunk apparently causes the runtime to deactivate all GPU threads for the basic chunk scheduler.

In terms of individual benchmark behavior, GEMM achieves the most speedup, which occurs with the static GPU-only configuration. While this schedule is not an adaptive, it is still facilitated by CoreTSAR, and for extremely GPU suitable applications can outperform the adaptive schedules. The CORR and COVAR benchmarks superficially behave similarly, but for a different reason. In their imbalanced workloads, each iteration i does $n - i$ units of work. Thus, they violate the assumption of the adaptive schedulers that the average work per iteration is constant. We expected one or more of the chunk schedulers would perform best in this scenario, but both CORR and COVAR are highly sensitive to overhead, and cannot tolerate the additional launches and copies of the chunk schedulers. Thus, the static schedulers (GPU and static) perform best in most cases. In the four GPU case for each, however, the split scheduler surges ahead. Split *stops using the CPU cores* and schedules across the GPUs in the three and four GPU cases. Our linear program does not handle varying time per iteration with heterogeneous hardware, but given relatively homogeneous hardware it handles the heterogeneous iterations much better. Using only GPUs, no CPU cores, with the Adaptive schedule achieves a further 10-20 percent performance improvement over the next best schedule in each case for CORR and COVAR.

Also unexpectedly, kmeans performs best with the basic chunk scheduler. With a precisely selected chunk value kmeans does quite well but, as Fig. 8 shows, its performance varies by as much as 50 percent across chunk sizes we tested. The adaptive schedulers are more robust in that they do not require users to search the input space in order to find a reasonable initial parameter.

Overall CoreTSAR scales well to at least four GPUs without loop body or memory layout changes for GPU-amenable applications. Further, each scheduler is stronger for certain tasks than others, and the adaptive scheduler is the best overall choice, even with the best chunk sizes for chunk schedulers. It remains stable, and within approximately 10 percent of optimal for all amenable benchmarks with homogeneous iterations. For heterogeneous iterations, static and chunk are better options.

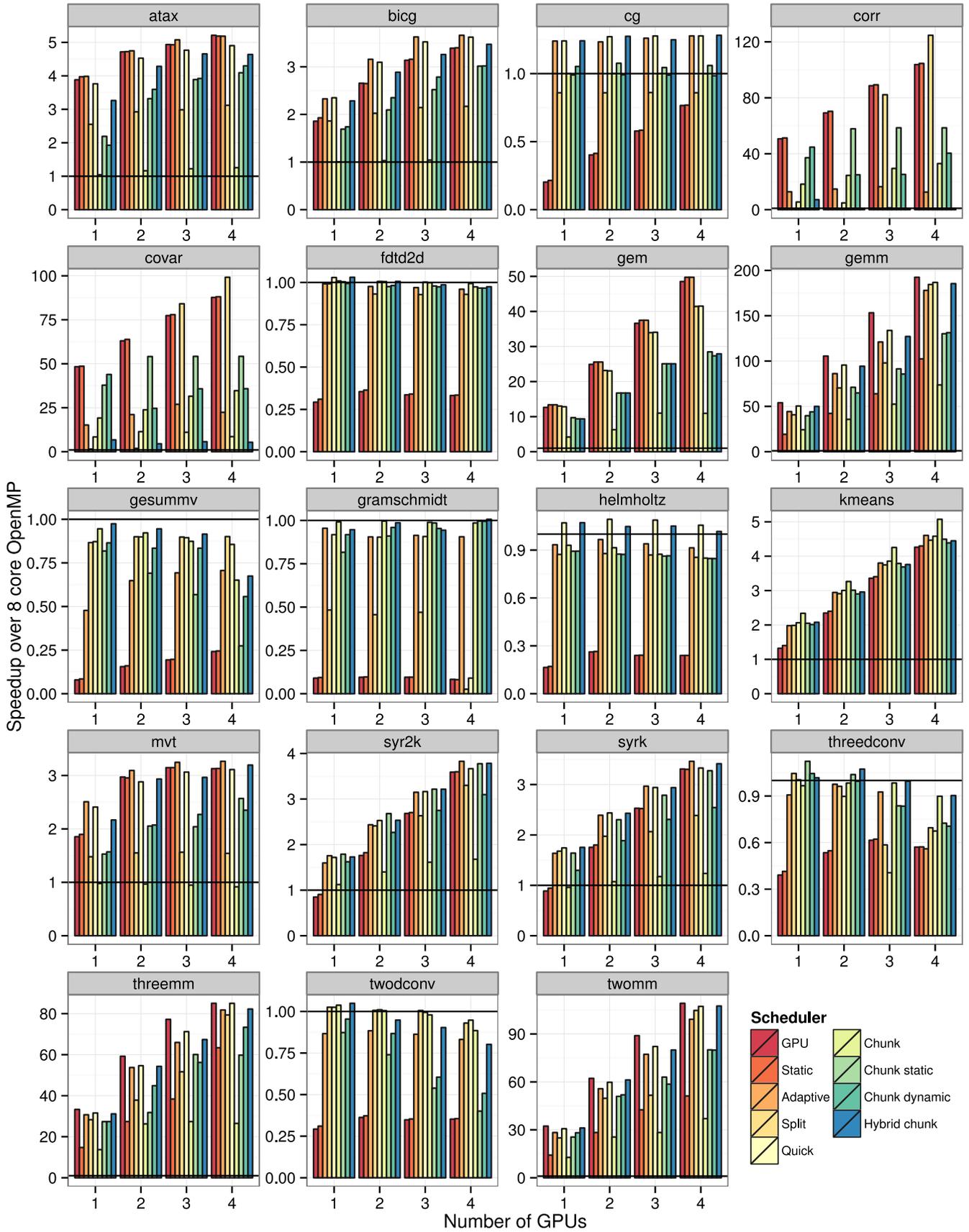


Fig. 9. Performance across schedulers and number of GPUs for all benchmarks, normalized to CPU OpenMP across eight cores.

5.3.2 GPU-Averse Applications

These are applications that *do not* run well on GPUs. Some are so sensitive to it that running any part of the job on a GPU causes slowdown. These are included to evaluate CoreTSAR's response to regions that should not use GPUs, or to running normally amenable applications on a system where the accelerator is particularly slow. While Jacobi solvers in general, and Helmholtz solvers in particular, are not GPU averse as a class, the implementation of Helmholtz that we evaluate is. Our Helmholtz is a generic CPU OpenMP version that runs correctly but slowly when compiled for the GPU. It never performs better by using a GPU for any work. This category also includes three PolyBench/GPU benchmarks (FDTD2D, GESUMMV and GRAMSCHMIDT). Each runs slower on a GPU than on one CPU or runs many passes, accentuating copy overhead.

In each case, schedulers that run more often, and thus convert the GPU threads to CPU threads faster, incur less performance loss. For the same reason, GPU-averse benchmarks that run many small passes perform better. For example, GESUMMV suffers more than the others by running 10 passes rather than 50 or thousands. For each of these benchmarks, the ability to convert GPU control threads to CPU threads is crucial. Without GPU backoff support, the total runtime of Helmholtz more than doubles for both adaptive and chunk based schedules, and as much as triples for the split schedule.

Three other benchmarks (CG, THREEEDCONV, and TWODCONV) fall into this category, but only marginally. Each can benefit from the first GPU. GPUs complete iterations faster than CPUs for these benchmarks, but they only have enough work to saturate a single GPU, or face increasing data transfer overhead as more are added. CG passes through the region enough times (1,900) that all but one GPU are converted to CPU threads very early in the computation, so it achieves roughly constant performance from one to four GPUs. The convolution codes do not run long enough to hide the overhead of extra GPUs enabled in the first few passes and show degrading performance.

5.4 Adaptation Across Machines

We now evaluate CoreTSAR's performance across several disparate systems. All systems run the same OS image and execute identical binaries for all tests. Table 1 lists the hardware in each system in detail. Of particular interest are the GPU-centric system `amdlow3`, which contains a dual-core Intel Celeron processor and NVIDIA C2050 GPU, and the CPU-centric system `armor1` with two quad-core Intel Xeon cores and a low power NVIDIA GT 520 GPU.

As some of our benchmarks require more memory than the smaller GPUs possess, we selected a representative subset (CG, GEM, kmeans, and SYR2K) with problem sizes that fit onto all evaluated GPUs. Fig. 10 shows results for these benchmarks across all five test platforms. The most prominent feature of the results across systems is the significant change in overall speedup. In particular, `amdlow3` exhibits consistently high speedups using the GPU, partly due to the extreme imbalance between its Intel Celeron processor and NVIDIA C2050 GPU. Even CG shows material speedups on `amdlow3`, as much as 2 \times . More importantly, even though

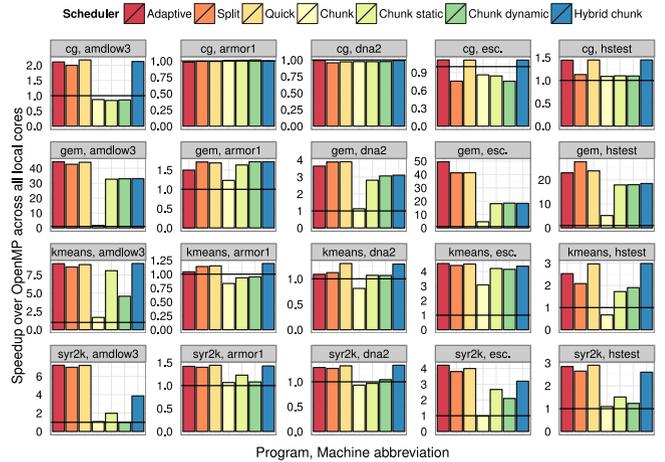


Fig. 10. CoreTSAR speedup across systems.

speedup and overall performance shift across the various systems for each benchmark, the distribution of performance by scheduler is similar. Thus, the right CoreTSAR scheduling algorithm is more related to the application than the hardware. Allowing the scheduler to be determined once per region, rather than once per machine. Further, these results show that the default adaptive scheduler is effective across hardware configurations, with only GEM as an issue, as a result of its single iteration. GEM's strong performance on the other devices also showcases the portability of our computed default division of work, which for that application is consistently near the best.

5.5 Comparison with Blocked Task Schedulers

In order to compare CoreTSAR's scheduling with a state of the art heterogeneous task scheduler, we employ those designed to support blocked task models. Specifically we port three benchmarks (GEMM, kmeans, and Helmholtz) to two freely available implementations of this type of model, `OmpSs` and `StarPU`. As with Accelerated OpenMP and CoreTSAR, we use the most straightforward port possible, transforming only the loop regions that CoreTSAR targets. For example, Fig. 1 lists a literal transcription of the GEMM implementation on `OmpSs`, calling functions defined in Fig. 1.

In order to provide an accurate comparison, the CoreTSAR codes evaluated here use the CUDA and C functions created for `OmpSs` and `StarPU` rather than using Accelerated OpenMP. In fact these functions were compiled into a single object file with `nvcc` that was then linked with the CoreTSAR, `OmpSs` and `StarPU` scheduling code, thus all three are scheduling over *identical* compute kernels. The `OmpSs` version was run with the versioning-stack scheduler, to support alternative implementations, as well as flags to allow prefetching and overlapping of data transfers for benchmarks where these offered speedup (slowdown was observed in one case). The `StarPU` implementations used the "dmda" scheduler with the history-based performance model, trained on at least 10 runs before results were collected.

GEMM and Helmholtz run each row of the main outer loop as an individual task. The outer loop for kmeans is fine grained, so we block it into chunks of 1,000 iterations for

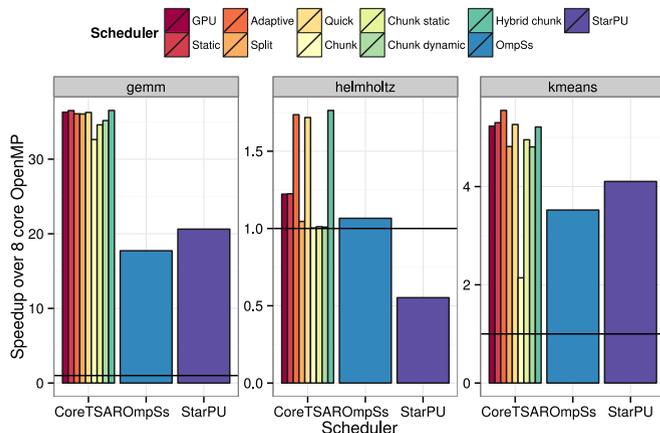


Fig. 11. Comparison of CoreTSAR with OmpSs and StarPU.

OmpSs and StarPU, and also use 1,000 iteration chunks as the default for CoreTSAR’s *chunk* schedulers although we allow it to adapt at runtime where capable. Each only copies the data necessary for a given task. For example, we only request the three rows necessary for a given Helmholtz row. We also disable CoreTSAR’s persistent memory support, since OmpSs does not provide an equivalent feature, though StarPU does.

Fig. 11 presents the speedup results, calculated as speedup over all eight CPU cores with the OpenMP dynamic schedule, with OmpSs and StarPU on the far right. While unrelated to the performance comparison, Helmholtz shows a performance benefit using GPUs in this case. In truth, the CPU version compiled with gcc is significantly slower (9 \times) than the version evaluated earlier, while the CUDA and OpenACC versions perform similarly.

Each of StarPU and OmpSs are block schedulers, operating much like our *Chunk* scheduler, and so we expect that they would perform similarly. The expectation holds for Helmholtz, wherein OmpSs performs almost identically to CoreTSAR’s *Chunk* scheduler with StarPU trailing by roughly 50 percent. In kmeans and GEMM each performs quite differently, with OmpSs and StarPU outperforming *Chunk* on kmeans and being heavily outperformed by it in GEMM.

While the computation and data transfers are nearly identical between the schedulers, the performance of CoreTSAR using one of the granularity adapting schedulers is consistently higher due to reduced overheads. Since CoreTSAR never explicitly creates the individual tasks, it never pays the cost to allocate or to initialize them, only paying for the aggregate tasks it runs. This benefit is especially noticeable in GEMM where CoreTSAR is 3 \times faster than OmpSs and 2 \times faster than StarPU scheduling the same work. Given the ability to adapt task granularity at runtime, all three would yield similar performance. It may be worthwhile to consider adding CoreTSAR, or a similar task-splitting design, to each of OmpSs and StarPU to reduce overhead for this type of computation.

6 RELATED WORK

With the proliferation of GPUs and other computational accelerators, several programming models and task schedulers have been proposed specifically for these environments.

In addition to the blocked task schedulers, StarPU [15], [16] and OmpSs [7], [17], which we discussed in Section 2, other designs have been proposed. Two major factors distinguish our work from these schedulers. First, they schedule at the granularity of discrete tasks, which in each case is defined by a function call, and forces the user to select the appropriate granularity of work even within a group of related tasks. Second, they require that the task functions are implemented in terms of blocks of data. These blocks generally need to be contiguous chunks of data, for common cases StarPU offers “filters” as a convenient way to divide data into equal size chunks, and recent work on OmpSS [18] has added support for potentially non-contiguous rectangular regions to be passed to tasks. With CoreTSAR, a task granularity may optionally be used, but is not required and often does not result in the best division of work. As to data blocks or transformation of tasks to operate on them, CoreTSAR handles unblocked accelerated OpenMP code, preserving the semantics of the original parallel region.

More relevant are the approaches taken by Qilin [19] and the scheduling framework presented by Ravi et al. [20], [21]. These authors present novel heterogeneous programming APIs that support adaptive scheduling between CPUs and a GPU. The Qilin API is in the form of a C++ template library that operates on special array structures and allows runtime generation of CPU and GPU code. Ravi et al.’s work generates CPU and GPU code from generalized reduction specifications. Both require reimplementing of existing codes in the associated model, constrain the adaptive scheduling approach to that used by the respective system, and target only one GPU. Qilin uses an adaptive approach similar to the one that we used in our previous work on Splitter [10] to support one GPU. However, they calculate the division in a training pass and simply reuse it in latter runs. The framework by Ravi et al. uses a chunk-based mechanism, with an option to combine chunks for scheduling on the GPU much in the way our dynamic chunk schedule does. Alternatively, CoreTSAR handles memory movement and adaptive scheduling of work while preserving existing code inside the region. Further it supports a range of scheduling mechanisms allowing a user to select an adaptive or chunk-based approach on a per region basis, as well as supporting an arbitrary number of arbitrarily capable GPUs and CPUs.

Our adaptive scheduling policies are also highly related to the approach taken by Ayguadé et al. [22] in looking for an alternative to the `schedule` clause in OpenMP. Rather than employing dynamic, or chunk style scheduling, they proposed the use of a learning scheme to do a static split. Their specific prediction methods and targets were different from ours, but their assertion that the adaptive policies sometimes benefited CPUs as well may be another reason to incorporate something like our adaptive schedules into OpenMP.

7 CONCLUSION

We have presented the design and implementation of CoreTSAR (Task-Size Adapting Runtime). We make four primary contributions: the design of our scheduler for adaptive scheduling across arbitrary numbers of heterogeneous devices; an implementation and optimization of

that design; the design and evaluation of seven adaptive scheduling policies; and our evaluation across four scientific codes, 15 benchmark kernels and a side-by-side comparison with OmpSs and StarPU. We achieve speed-ups as high as $3.74\times$ over the best performance that uses all cores and a single GPU. When compared to the original CPU performance on eight cores, we achieve as much as $180\times$ for one benchmark. Further, we present an extension to our memory management system that transparently aligns matrices during mapping, improving performance in some cases by as much as $2.5\times$. These results clearly demonstrate the benefits to be gained from runtime adaptation of task sizes and motivate the addition of a co-scheduling interface, such as the `hetero()` clause that we propose, to Accelerated OpenMP.

As future work, we will investigate more comprehensive memory association support. Starting from the padding transformation we presented here, we will pursue more automatic transformations to allow loop body code to reference different memory layouts transparently. In the main scheduler, CoreTSAR could automatically detect NUMA issues, and the association of GPUs to CPUs and manage these automatically for greater performance. Finally, the memory management interface that we present is the first step towards a general interface for declaring the relationship between tasks and the portions of inputs and outputs that they require. Given that information, many schedulers, including ours, could automatically manage input and output, providing significant value especially as computers become more complex.

ACKNOWLEDGMENTS

This material is based upon work supported by the US Department of Energy's Lawrence Livermore National Laboratory; Office of Science, under Award number DE-AC52-07NA27344; Office of Advanced Scientific Computing Research (LLNL-JRNL-662817); the Air Force Office of Scientific Research (AFOSR) Computational Mathematics Program via Grant No. FA9550-12-1-0442; NSF I/UCRC IIP-1266245 via the NSF Center for High-Performance Reconfigurable Computing (CHREC); and a DoD National Defense Science & Engineering Graduate Fellowship (NDSEG).

REFERENCES

- [1] J. C. Beyer, E. J. Stotzer, A. Hart, and B. R. de Supinski, "OpenMP for Accelerators," in *Proc. 7th Int. Workshop OpenMP*, pp. 108–121 [Online]. Available: http://link.springer.com/chapter/10.1007/978-3-642-21487-5_9, 2011.
- [2] M. Wolfe. (2010, Mar.). Implementing the PGI Accelerator Model. *Proc. Annu. Workshop General Purpose Process. Graph. Process. Units* [Online]. Available: <http://portal.acm.org/citation.cfm?id=1735688.1735697&coll=DL&d1=GUIDE&CFID=53317199&CFTOKEN=95945713>
- [3] CAPS Enterprise, Cray Inc., NVIDIA and the Portland Group. (2011, Nov.) The OpenACC application programming interface, v1.0 [Online]. Available: <http://www.openacc-standard.org>
- [4] R. Dolbeau, S. Bihan, and F. Bodin, "HMPP: A hybrid multi-core parallel programming environment," in *Proc. Workshop General Purpose Process. Graph. Process. Units*, 2007.
- [5] CUDA programming guide. (2007) [Online]. Available: <http://docs.nvidia.com/cuda/cuda-c-programming-guide/>
- [6] The OpenCL specification. (2012, Nov.) [Online]. Available: <http://www.khronos.org/registry/cl/specs/opengl-1.2.pdf>
- [7] A. Duran, E. Ayguade, R. Badia, J. Labarta, L. Martinell, X. Martorell, and J. Planas, "OmpSs: A proposal for programming heterogeneous multi-core architectures," *Parallel Process. Lett.*, vol. 21, no. 2, pp. 173–193, 2011.
- [8] C. Augonnet, S. Thibault, R. Namyst, and P. Wacrenier, "StarPU: A unified platform for task scheduling on heterogeneous multi-core architectures," in *Proc. Euro-Par 2009 Parallel Process.*, 2009, vol. 5704, pp. 863–874.
- [9] T. R. W. Scogland, B. Rountree, W. Feng, and B. R. de Supinski, "CoreTSAR: Adaptive worksharing for heterogeneous systems," in *Proc. Int. Supercomput. Conf.*, 2014, pp. 172–186.
- [10] T. R. W. Scogland, B. Rountree, W. Feng, and B. R. de Supinski. (2012, May). Heterogeneous task scheduling for accelerated OpenMP. *Proc. Int. Parallel Distrib. Process. Symp.*, pp. 144–155 [Online]. Available: <http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=6267831&contentType=Conference+Publications&matchBoolean%3Dtrue%26rowsPerPage%3D30%26searchField%3DSearch+All%26queryText%3D%28p+Title%3A%22Heterogeneous+Task+Scheduling+for+Accelerated+OpenMP%22%29>
- [11] S. Grauer-Gray, L. Xu, R. Searles, S. Ayalasomayajula, and J. Cavazos. (2012). Auto-Tuning a high-level language targeted to GPU codes. *Proc. Innovative Parallel Comput.*, pp. 1–10 [Online]. Available: <http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=6339595&contentType=Conference+Publications&matchBoolean%3Dtrue%26rowsPerPage%3D30%26searchField%3DSearch+All%26queryText%3D%28p+Title%3A%22Auto-tuning+a+High-Level+Language+Targeted+to+GPU+Codes%22%29>
- [12] D. H. Bailey, E. Barszcz, J. Barton, D. Browning, R. Carter, L. Dagum, R. Fatoohi, P. Frederickson, T. Lasinski, R. Schreiber, H. Simon, V. Venkatakrishnan, and S. Weeratunga. (1991). The NAS parallel benchmarks summary and preliminary results. *Proc. Int. Conf. High Perform. Comput., Netw., Storage Anal. (SuperComput.)*, pp. 158–165 [Online]. Available: <http://portal.acm.org/citation.cfm?id=125826.125925>
- [13] R. Anandakrishnan, T. R. W. Scogland, A. T. Fenley, J. C. Gordon, W. Feng, and A. V. Onufriev. (2010, Jun.). Accelerating electrostatic surface potential calculation with multi-scale approximation on graphics processing units. *J. Mol. Graph. Model.* [Online]28(8), pp. 904–910. Available: <http://www.sciencedirect.com/science/article/pii/S1093326310000537>
- [14] M. Daga, T. R. W. Scogland, and W. Feng. (2011). Architecture-aware mapping and optimization on a 1600-core GPU. *Proc. Int. Conf. Parallel Distrib. Syst.*, pp. 316–323 [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6121293
- [15] C. Augonnet, S. Thibault, R. Namyst, and P.-A. Wacrenier. (2009, Aug.). StarPU: A unified platform for task scheduling on heterogeneous multicore architectures. *Proc. Int. Euro-Par Conf. Parallel Process.* [Online]. Available: <http://www.springerlink.com/index/h013578235633mw3.pdf>
- [16] C. Augonnet, S. Thibault, and R. Namyst. (2010, Mar.). StarPU: A runtime system for scheduling tasks over accelerator-based multi-core machines. Laboratoire Bordelais de Recherche en Informatique (LaBRI), RUNTIME (INRIA Bordeaux - Sud-Ouest), Tech. Rep. RR-7240 [Online]. Available: <http://hal.inria.fr/inria-00467677>
- [17] J. Bueno, J. Planas, A. Duran, R. Badia, X. Martorell, E. Ayguade, and J. Labarta, "Productive programming of GPU clusters with OmpSs," in *Proc. 26th IEEE Int. Parallel Distrib. Process. Symp.*, 2012, pp. 557–568.
- [18] J. Bueno, X. Martorell, R. Badia, E. Ayguade, and J. Labarta. (2013). Implementing OmpSs support for regions of data in architectures with multiple address spaces. *Proc. Int. Conf. Supercomput.*, pp. 359–368 [Online]. Available: <http://dl.acm.org/citation.cfm?doid=2464996.2465017>
- [19] C.-K. Luk, S. Hong, and H. Kim. (2009, Dec.). Qilin: Exploiting parallelism on heterogeneous multiprocessors with adaptive mapping. *Proc. 42nd Annu. IEEE/ACM Int. Symp. Microarchit.* [Online]. Available: <http://portal.acm.org/citation.cfm?id=1669121>
- [20] V. T. Ravi and G. Agrawal, "A dynamic scheduling framework for emerging heterogeneous systems," in *Proc. 18th Int. Conf. High Perform. Comput.*, 2011, pp. 1–10.
- [21] V. T. Ravi, W. Ma, D. Chiu, and G. Agrawal, "Compiler and runtime support for enabling generalized reduction computations on heterogeneous parallel configurations," in *Proc. 24th ACM Int. Conf. Supercomput.*, Jun. 2010, pp. 137–146.

- [22] E. Ayguadé, B. Blainey, A. Duran, J. Labarta, F. Martínez, X. Martorell, and R. Silvera, "Is the schedule clause really necessary in OpenMP?" in *Proc. Workshop OpenMP Appl. Tools.*, Jun. 2003, pp. 147–159.



Thomas R.W. Scogland received the BS degree in computer science from Purdue University in 2007, a NDSEG Graduate Fellowship in 2009, and the MS degree from Virginia Tech in 2012. He is currently working toward the PhD degree in the Department of Computer Science at Virginia Tech (VT), where he is a member of the Synergy Lab. His primary research area is in high-performance computing, with a focus on scheduling in heterogeneous systems and green computing. He is a student member of the ACM and IEEE.



Wu-Chun Feng received the BS degrees in computer engineering and music (honors) and the MS degree in computer engineering from Penn State University in 1988 and 1990, respectively. He received the PhD degree in computer science from the University of Illinois at Urbana-Champaign in 1996. He is the Elizabeth & James E. Turner fellow and a professor of computer science, electrical & computer engineering, and health sciences at Virginia Tech (VT), where he also directs the Synergy Laboratory. Grassroots

projects that he leads include the Green500, Supercomputing in Small Spaces, and MyVICE. His research interests encompass a broad range of topics in efficient parallel and distributed computing, including high-performance computing and networking, energy-efficient (or green) supercomputing, heterogeneous and GPU computing, cloud and grid computing, MOON computing, bioinformatics, and computer science pedagogy for K-12. He is a distinguished member of the ACM and a senior member of the IEEE.



Barry Rountree received the BA degree in theater arts and drama from the Ohio University Honors Tutorial College, the MS degree in network and system administration from Florida State University, and the PhD degree in computer science from the University of Arizona. His current work focuses on optimizing massively parallel performance under hard electrical power bounds, particularly with regard to exascale system designs.



Bronis R. de Supinski is the chief technology officer (CTO) for Livermore Computing (LC) at Lawrence Livermore National Laboratory (LLNL). In this role, he is responsible for formulating LLNL's large-scale computing strategy and overseeing its implementation. His research has explored topics including programming models, algorithms, performance, code correctness and resilience for future large scale systems. He currently continues his interests in these topics, particularly programming models, and serves as the chair of the OpenMP Language Committee. Throughout his career, he received several awards, including the prestigious Gordon Bell Prize in 2005 and 2006, as well as an R&D 100 for his leadership of a team that developed a novel scalable debugging tool. He is a member of the ACM and the IEEE Computer Society.

▷ For more information on this or any other computing topic, please visit our Digital Library at www.computer.org/publications/dlib.