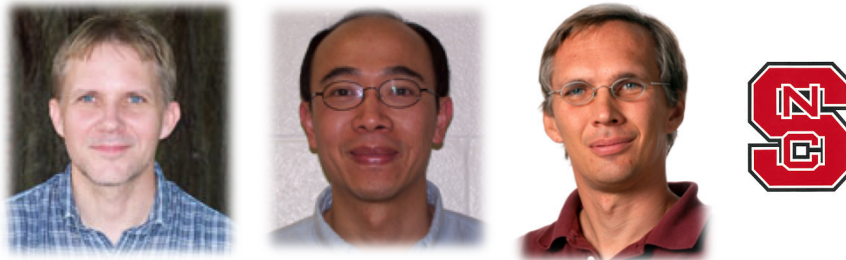


Co-Design of Hardware/Software for Predicting MAV Aerodynamics



E. de Sturler, **W. Feng**, C. Roy, A. Sandu, D. Tafti



J. Edwards, H. Luo, F. Mueller

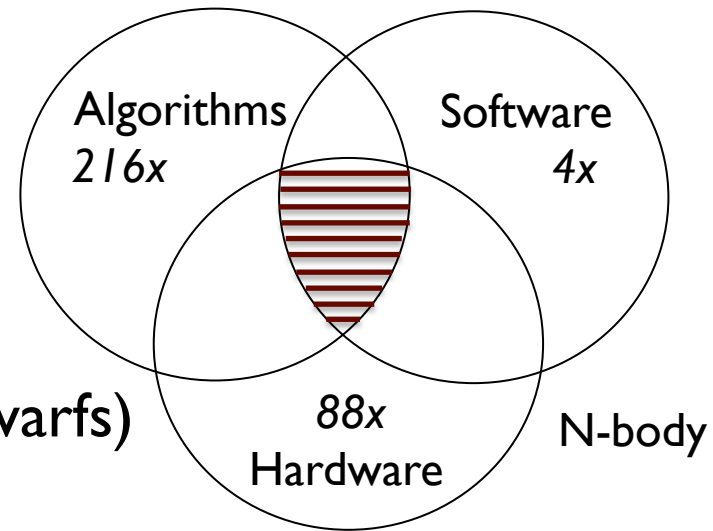


Fariba Fahroo, Computational Mathematics



Vision

- Synergistic co-design process for the *structured/unstructured grid motifs* (or dwarfs) in computational fluid dynamics (CFD) to support aerodynamic predictions for micro-air vehicles (MAVs).
 - Malleable **algorithms**
 - ... that can be mapped and optimized in **software**
 - ... onto the right type of processing core in **hardware**
 - ... at the right time
 - Co-design feedback to vendors to assist in guiding future hardware design



Synergistic Co-Design: Enabling and Empowering

Synergy Lab. | CS @ VT | Virginia Tech | NCSU

AFOSR-BRI

synergistic co-design towards an ecosystem for heterogeneous parallel computing

Navigation

- Home
- Co-design Approach
- CFD Codes
- Resources
 - Publications
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 - Visualizations
- Affiliates
- People
- Contact

Last updated

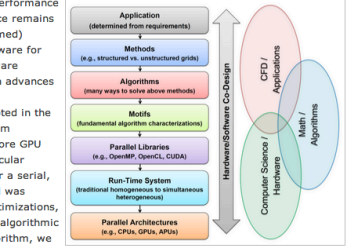
February 04, 2014

Our research has been sponsored by:



Overview
25 July, 2013

While Moore's Law theoretically doubles processor performance every 24 months, much of the realizable performance remains untapped because the burden falls to the (less informed) domain scientist or engineer to exploit parallel hardware for performance gains. Even when such untapped hardware potential is fully realized, it is often not coupled with advances in algorithmic innovation, which can deliver further (multiplicative) speed-up beyond Moore's Law, as noted in the **AFOSR BAA**. For example, in a heterogeneous system containing a CPU and GPU, a straightforward 1600-core GPU parallelization of a CPU-based n-body code for molecular modeling resulted in only an 88.4-fold speed-up over a serial, but SSE-vectorized, CPU code. An additional 4.2-fold was extracted when applying architecture-aware GPU optimizations, resulting in a 371-fold speed-up. By also leveraging algorithmic innovation via a hierarchical charge partitioning algorithm, we delivered an additional 216-fold speed-up, resulting in a multiplicative speed-up of 80,000-fold.



We propose to expand the aforementioned notion of hardware/software co-design heterogeneity in hardware, through the systems software and middleware

Together, the results are mapped and the magnitude better...
major artifact... computational mot... system will en... can better fo...

Hardware/software co-design...
processing core...
ecosystem for...
in CFD in supp...
inue working w...
rather than th...

VirginiaTech *Scholar*
Invent the Future a service of Learning Technologies

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CS Systems Search 201... ▾ D.I.G. (D.o.D. Intere... ▾ Interdisciplinary Gra... ▾ More Sites ▾

Home

- Announcements
- Calendar
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- Wiki

AFOSR Co-Design BRI 2012

Options

Site to foster collaboration on the 2012 AFOSR Basic Research Initiative (BRI) grant on Co-Design of CFD codes/hardware.

Place announcements under Announcements (left). The most recent announcements will then appear under Recent Announcements (right).

- Place documents under Resources (left) and try to give them a reasonable name (and perhaps version number),
- We can use the wiki (left) to communicate, discuss, post ideas.
- You can send email to all by emailing the site list: codesign2012@scholar.vt.edu (note: you may need to go

Recent Announcements

Options

Announcements (viewing announcements from the last 10 days)

There are currently no announcements at this location.

Calendar

< Today >					
Mon	Tue	Wed	Thu	Fri	Sat
		2	3	4	5
	9	10	11	12	13
16	17	18	19	20	



Team @ &

CS : Computer Science
Math : Mathematics
AOE/MAE : Aerospace & Ocean
Engg/Mechanical & Aerospace Engg.

- Virginia Tech (5 PIs + 7 students/staff)
 - Eric de Sturler Numerical Methods (solvers & preconditioners)
 - Wu Feng, Lead PI Parallel Computing (performance, programmability, portability)
 - Chris Roy CFD (structured grid and ALE mesh movement)
 - Adrian Sandu Numerical Methods (time stepping & discretization)
 - Danesh Tafti CFD (pressure-based multiblock structured)
 - Research Scientist (1), Postdocs (1), and Graduate Students (5)
- North Carolina State University (3 PIs + 3 students/staff)
 - Jack Edwards CFD (multiblock structured w/ implicit solvers)
 - Hong Luo CFD (unstructured grid / compressible)
 - Frank Mueller Parallel Computing (languages, compilers, scalability)
 - Postdocs (1), Graduate Students (2)

Interdisciplinary Collaboration

(via formal biweekly meetings + informal meetings)

CS : Computer Science

Math : Mathematics

AOE/MAE : Aerospace & Ocean

Engg/Mechanical & Aerospace Engg.

Eric de Sturler

Jack Edwards

Wu Feng

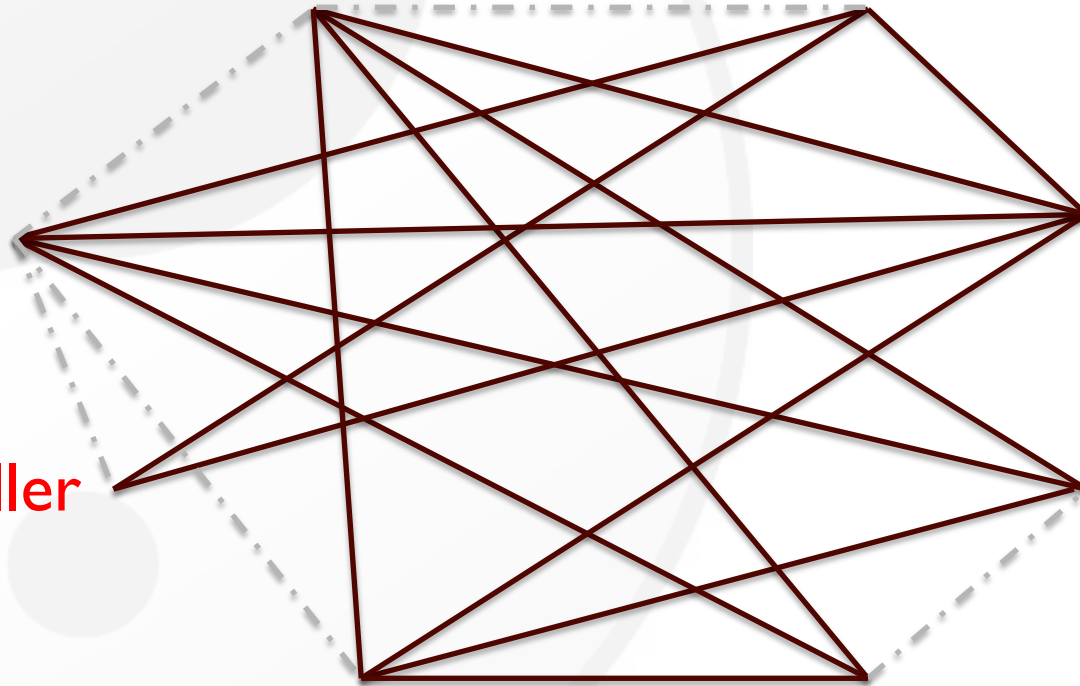
Hong Luo

Frank Mueller

Chris Roy

Adrian Sandu

Danesh Tafti

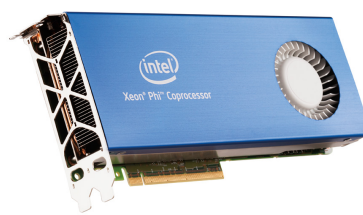


Why Synergistic Co-Design? Why Now?

- Increasing heterogeneity in computing resources



Altera FPGA



Intel MIC



NVIDIA GPU



TI DSP

... across a wide variety of environments



Heterogeneous Systems in HPC

- Statistics

- Four out of top 10 systems
- Performance share in Top500 systems 5% (2009) → 35% (2013)

- HokieSpeed

- CPU+GPU heterogeneous supercomputer with large-scale visualization wall
- Debuted as the GREENEST commodity supercomputer in the U.S. in Nov. 2011



HokieSpeed Viz Wall (Eight 46" 3D HDTVs)

1	Tianhe-2 (MilkyWay-2) - TH-IVB-FEP Cluster, Intel Xeon E5-2692 Intel Xeon Phi 31S1P
2	Titan - Cray XK7 , Opteron 6274 NVIDIA K20x
3	Sequoia - BlueGene/Q, Power BQC 16C 1.60 GHz, Custom IBM
4	K computer, SPARC64 VIIIfx 2.0GHz, Tofu interconnect Fujitsu
5	Mira - BlueGene/Q, Power BQC 16C 1.60GHz, Custom IBM
6	Piz Daint - Cray XC30, Xeon E5-2670 8C 2.70GHz NVIDIA K20x
7	Stampede - PowerEdge C8220, Xeon E5-2680 8C 2.70GHz Intel Xeon Phi SE10P
8	JUQUEEN - BlueGene/Q, Power BQC 16C 1.600GHz, Custom Interconnect IBM
9	Vulcan - BlueGene/Q, Power BQC 16C 1.600GHz, Custom Interconnect IBM
10	SuperMUC - iDataPlex DX360M4, Xeon E5-2680 8C 2.70GHz, Infiniband FDR



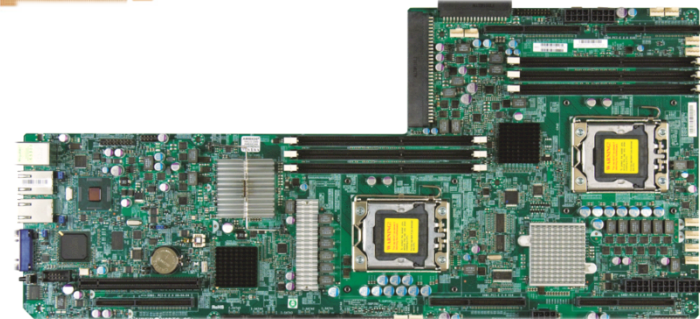
A GPU-Accelerated Supercomputer for the Masses

- Hardware

- Total Nodes: 209, where each compute node consists of
 - Motherboard: Supermicro 2026GT-TRF Dual Intel Xeon
 - CPUs: Two 2.4-GHz Intel Xeon E5645 6-core (12 CPU cores per node)
 - GPUs: Two NVIDIA Tesla Fermi GPUs (M2050/C2050)

- Software

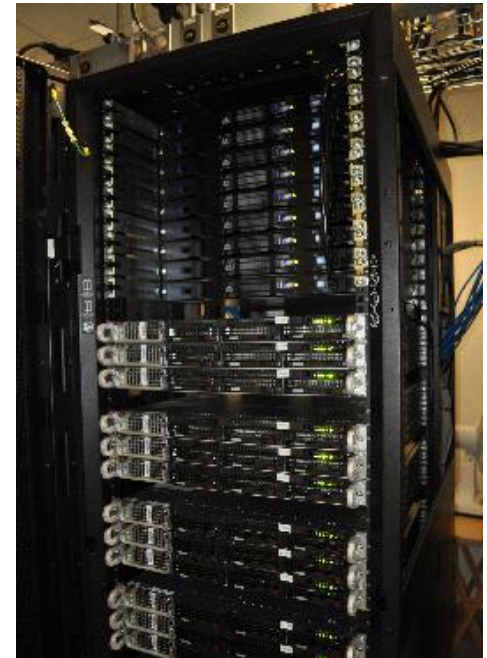
- CUDA 4.1.28, 5.0.35, 6.5.14
via module load/unload
- PGI compilers v13.4
w/ CUDA Fortran & OpenACC support
- OpenMPI & MVAPICH2-1.9
- Torque/Maui job management system



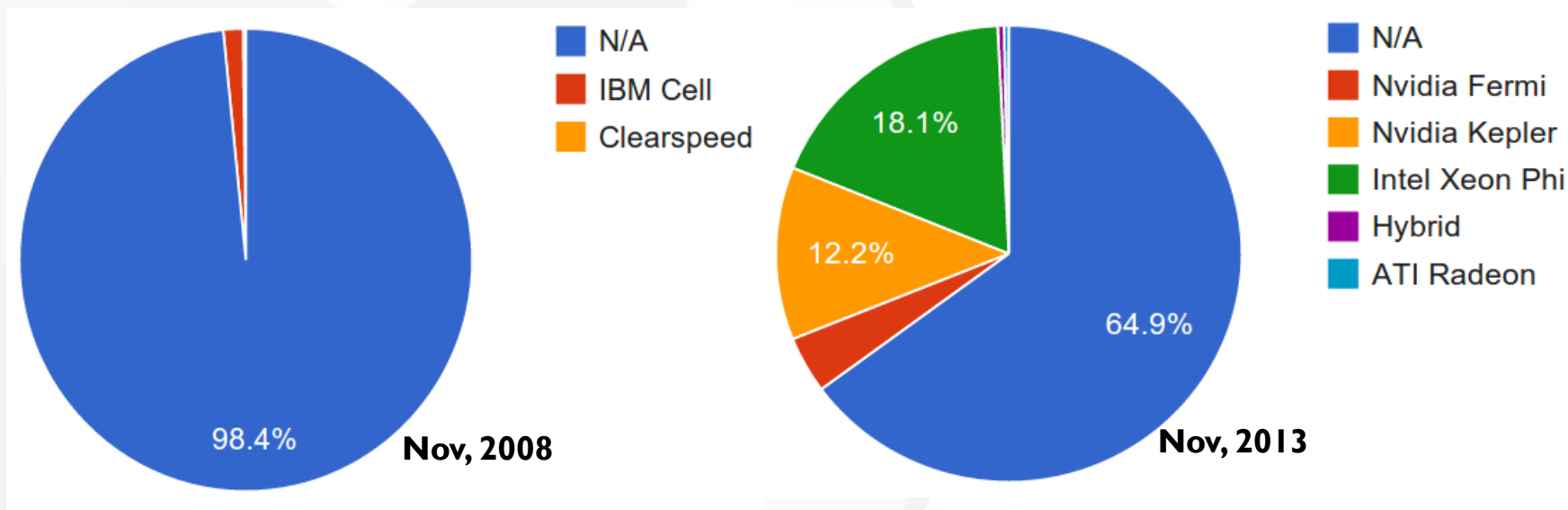
ARC Cluster



- Hardware
 - 2x AMD Opteron 6128 (8 cores each)
 - 108 nodes = 1728 CPU cores
 - NVIDIA GTX480, GTX680 , C2050, K20c: 108 GPUs
 - Mellanox QDR InfiniBand: 40Gbit/s
- Software
 - CUDA 5.0
 - PGI Compilers V13.4 w/ CUDA Fortran & OpenACC support
 - OpenMPI & MVAPICH2-1.9 w/ GPUDirect V2 capability
 - Torque/Maui job management system

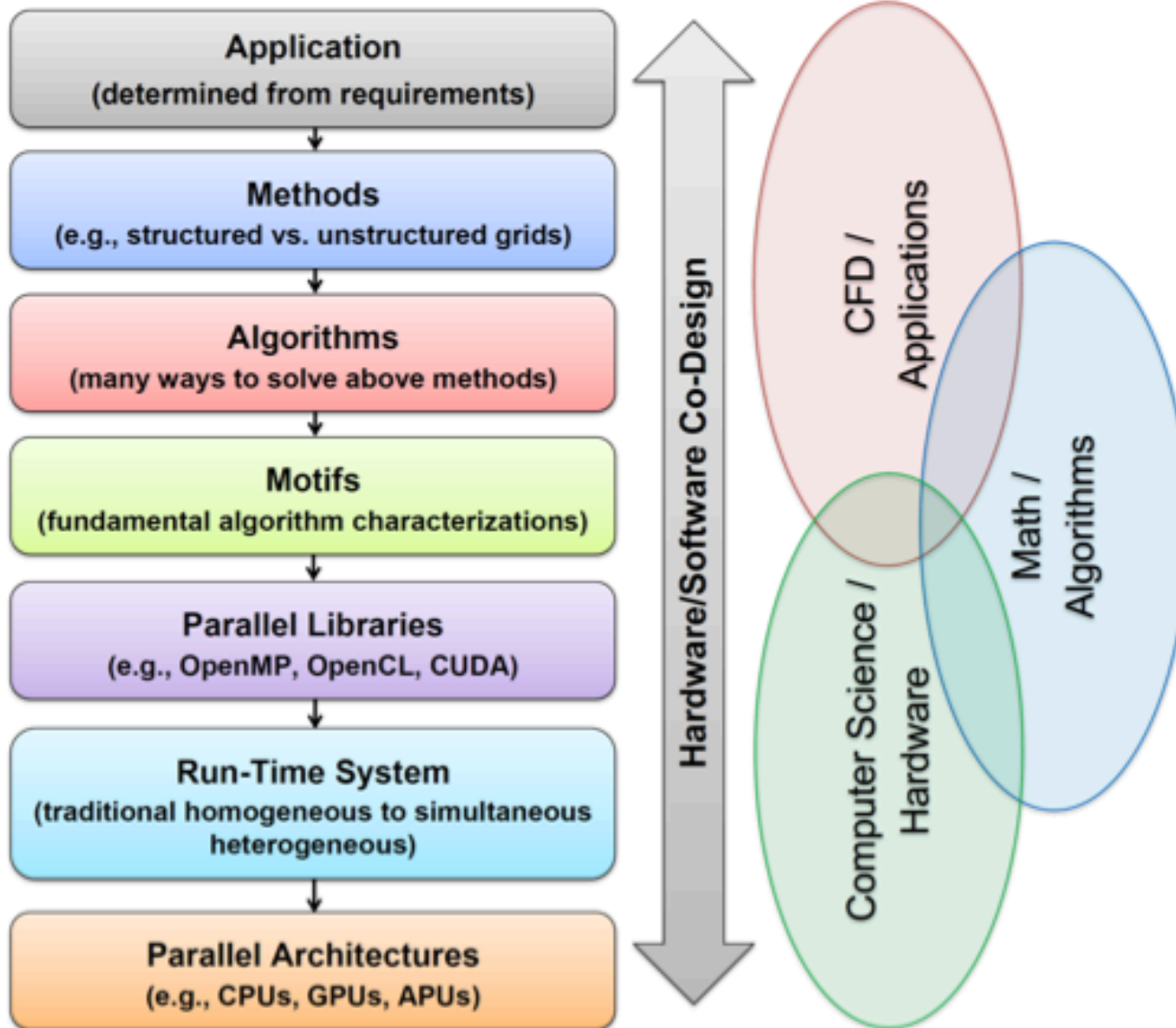


Diversity of Heterogeneous Systems

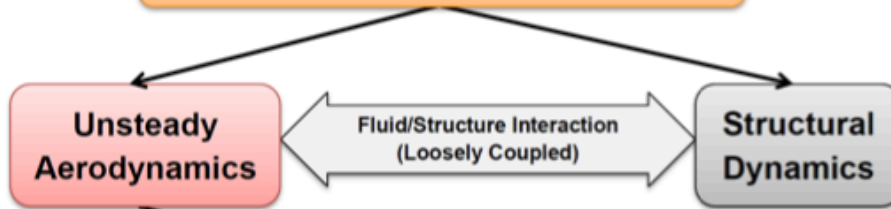


Performance Share of Accelerators in Top500 Systems

Layered Co-Design



Micro Air Vehicles (MAVs)



Incompressible Flow Method

Grid Type

Spatial Discretization

Temporal Discretization

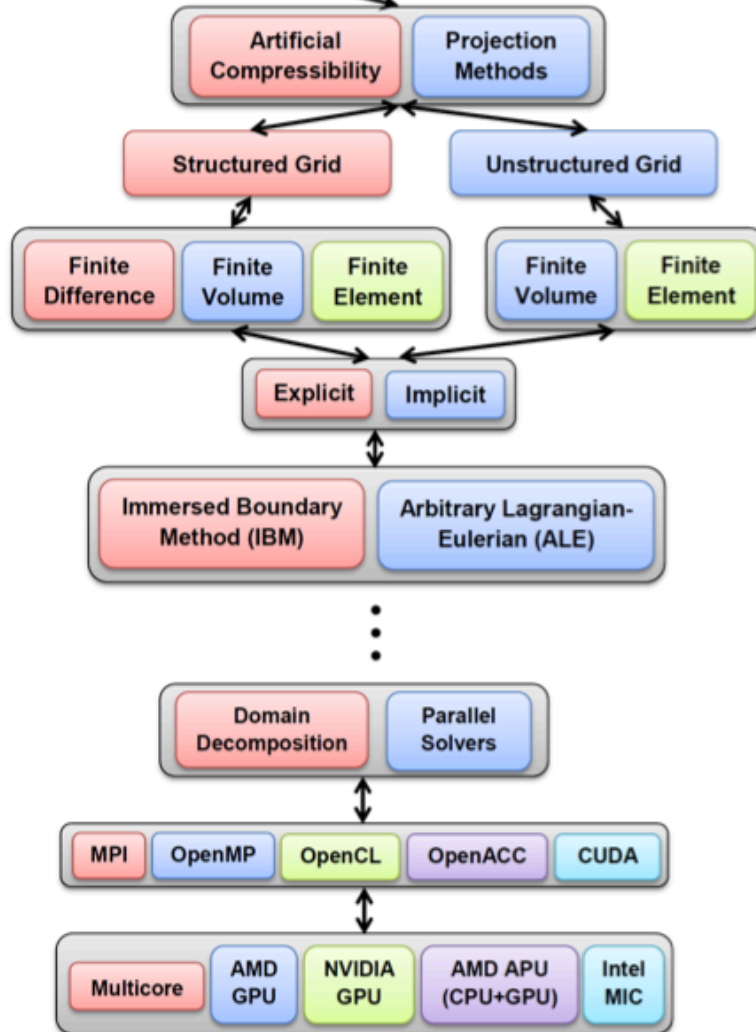
Structural Motion

⋮

Parallelism

Parallel Libraries

Parallel Architectures



Co-Design for Micro Air Vehicles (MAVs)

Micro Air Vehicles (MAVs)

**Unsteady Aero
(A, B, C, D)**

Fluid/Structure Interaction
(Loosely Coupled)

**Structural
Dynamics (TBD)**

Artificial Compressibility (B, D) Projection Methods (A) Higher-Order Methods (C)

Structured Grid (A, B, D) Unstructured Grid (C)

Finite Difference (D) Finite Volume (A, B, D) Finite Element (C)

Explicit (A, B, C, D) Implicit (A, B, C, D)

Immersed Boundary Method (A, B) Arbitrary Lagrangian-Eulerian (A, B, C)

MPI SnucL

MPI OpenMP OpenACC OpenCL CUDA

Multicore CPU AMD GPU NVIDIA GPU AMD APU (CPU+GPU) Intel MIC

Incompressible Flow Method

Grid Type

Spatial Discretization

Temporal Discretization

Structural Motion

⋮

Internode Parallelism

Intranode Parallelism

Target Parallel Architectures

CFD Codes

A

GenIDLEST: Struct, Press Project, FVM

B

INCOMP3D: Struct, Art Compr, FVM

C

RDGFLO3D: Unstr, FEM

D

SENSEI: Struct, Art Comp, FVM

Synergistic Co-Design
from 10,000 Feet:
Performance Perspective

Bat Wing Simulation for GenIDLEST Code

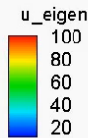
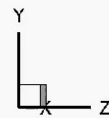
Amit Amritkar and Danesh Tafti, Dept. of Mechanical Engineering, Virginia Tech

GPU

CPU

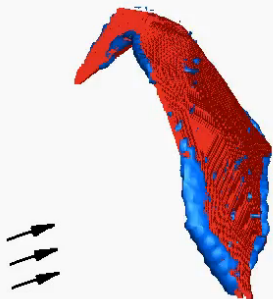
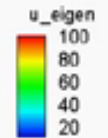
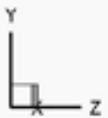
Simulation of bat wing using IBM

Amit Amritkar, Danesh Tafti



Simulation of bat wing using IBM

Amit Amritkar, Danesh Tafti



Wall Time = 0.000 minutes



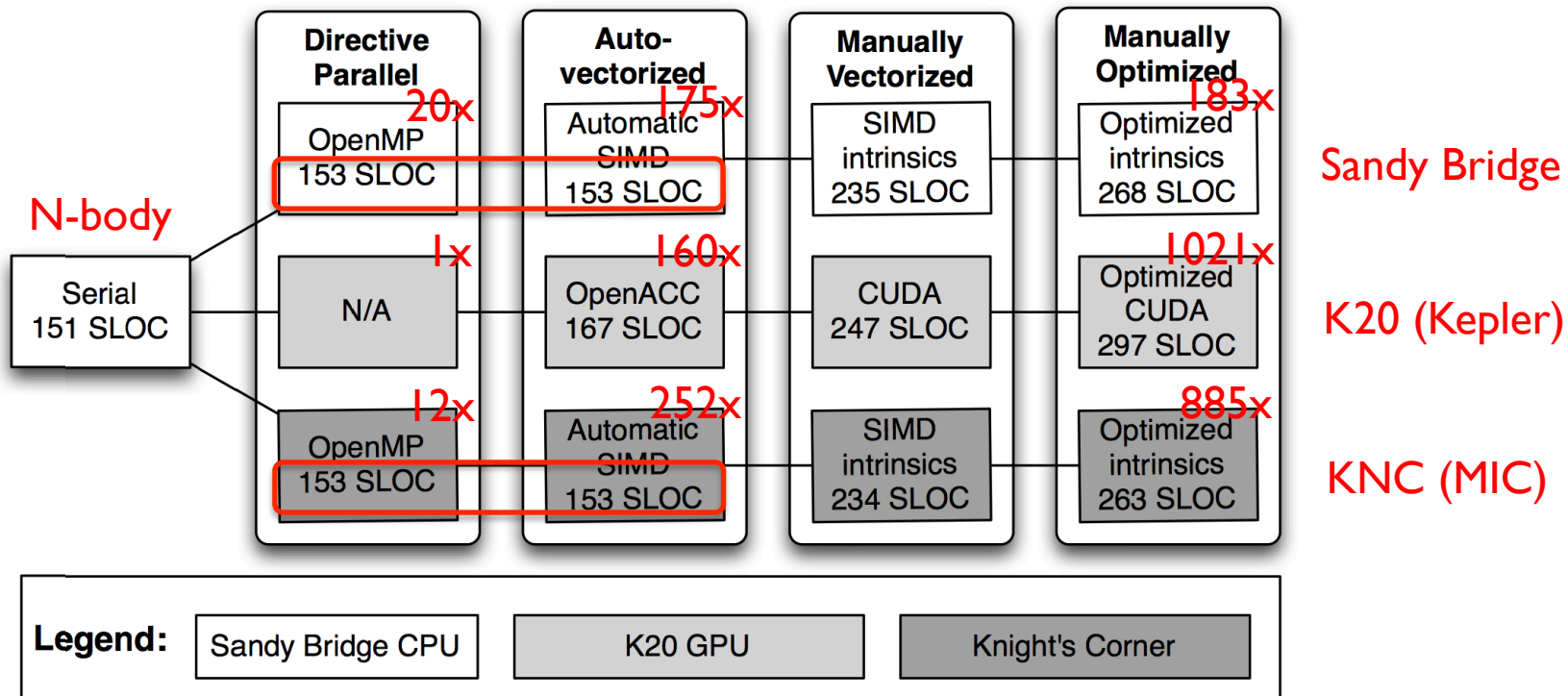
Wall Time = 0.000 minutes



Co-Design Around Three P's: Performance, Programmability, Portability

“Productivity = Performance + Programmability + Portability”

- Multi-dimensional optimization across two or more P's
- ... first *manual co-design* ... then *automated co-design*



What's Next?

- Two-Year Renewal Option for Years 4 and 5
- Brainstorming ...
 - Continue with the status quo?
 - Manual Co-Design for Each Code + Starchart + Stargazer
 - Multi-Dimensional Performance, Programmability, and Portability
 - Platforms, languages, run-time systems
 - Continued Extensions to MetaMorph
 - MetaMorph-Enabled CFD Codes
 - Explore (or add) new directions
 - Multi-Pronged Programming Language w/ Auto-Optimization Approach
 - Adaptive Run-Time System for Heterogeneous Computing
 - MetaMorph + ParMETIS? How? (Amit A.)
 - Something more radical?

Acknowledgements

- This work was funded by the Air Force Office of Scientific Research (AFOSR) Computational Mathematics Program
 - Program Manager: Fariba Fahroo
 - Grant No. FA9550-12-1-0442

