Objective

- 3DHP (3 integrated Heterogeneous Processors) is emerging as a key enabling tech for parallel and scalable heterogeneous computing.
- This project is to address thermal integrity issues in 3DHP (3 integrated Heterogeneous Processors) through synergy from a holistic cross-layer approach.
- Three target system layers include physical, architecture and runtime layers.

Approach

- The proposed approach has three major target 3DHP system layers.
- Three investigators with necessary background and expertise.
- Online temp/stress sensing measurements are utilized for adaptive error correction and HW/workload runtime interaction control.

Adaptive EDAC & Refresh

- Leakage power of DRAM cell is modeled to exponentially increase with temp.
- Cells affected by hotspots show lower retention time forcing higher global refresh frequency.
- Adaptive control of EDAC/refresh is proposed as a compromised solution.

Target Layer Thermal Reliability (Lead PI) Issue Proposed Approach

RunTime Layer
(B. Jang)
- Need for dynamic runtime management of thermal reliability of the target workload
- DTRM (dynamic thermal reliability management) for fine-grained runtime control of interaction between workload and HW resources

Architecture
(M. Choi)
- Spatially and temporally varying error rate induced by hotspots
- Adaptive EDAC (Error Detection & Correction) & DRAM refresh engine for reliable storage and transfer of data among CPU, GPU and DRAM dies via TSVs

Physical Layer (Y. Shi)
- Need for on-chip online sensing for thermal and mechanical integrity
- Distributed temperature and TSV stress co-sensor framework for 3D stacked CPU/GPU+DRAM heterogeneous processor

Dynamic Thermal Reliability Management

- To reduce the thermal hotspots and temperature gradients with minimal possible performance impact for local workloads on 3DHP
- Leveraging advanced techniques including DWGS (Dynamic Workgroup Scheduling), inherent redundancy (especially in GPU), DVFS (Dynamic Voltage Frequency Scaling), PG (Power Gating).

Current Progress

- A novel TSV temp/stress co-sensor has been designed and characterized.
- A 5-stage BCH decoder has been designed and implemented.
- DTRM framework has been implemented and integrated into multi2sim simulator for further study.

Current References


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